AK2572

APC for Burst Mode Applicable Direct Modulation Laser Diode

FEATURES

- Temperature compensation programming function (APC_FF) of Bias current (0~85mA) and Modulation current (0~10mA/0~2.2V) responding to the detected temperature by the On-chip temperature sensor.
- Stable feedback function in the digital scheme (APC_FB).
- SFP support TXFAULT function and 1k bit ID field (EEPROM User Area).
- LD Power leveling function by either Hardware pin control or Register setting.
- Various alarm functions of Optical output decline (OPTALM), Excessive LD current (CURRALM), Exceptional temperature (TEMPALM) and Irregular external signals (EXTALM1 and EXTALM2).
- Operation adjustment function via 2-wire Digital interface after assembled into sub-system.
- On-chip Oscillator allows a Self-running operation.
- Single 3.3 V [Typ.] power supply.

APPLICATIONS

For LD modules applied to Continuous and Burst mode

OUTLINES

The AK2572 enables to keep the optical power of the direct modulation LD (Laser Diode) constant by the APC (Automatic Power Control) circuit. It consists of a current programming function (APC_FF) responding to the temperature characteristics of each LD, and a Digital feedback function (APC_FB) to adjust the LD current based on the monitoring PD (Photo Diode) current.

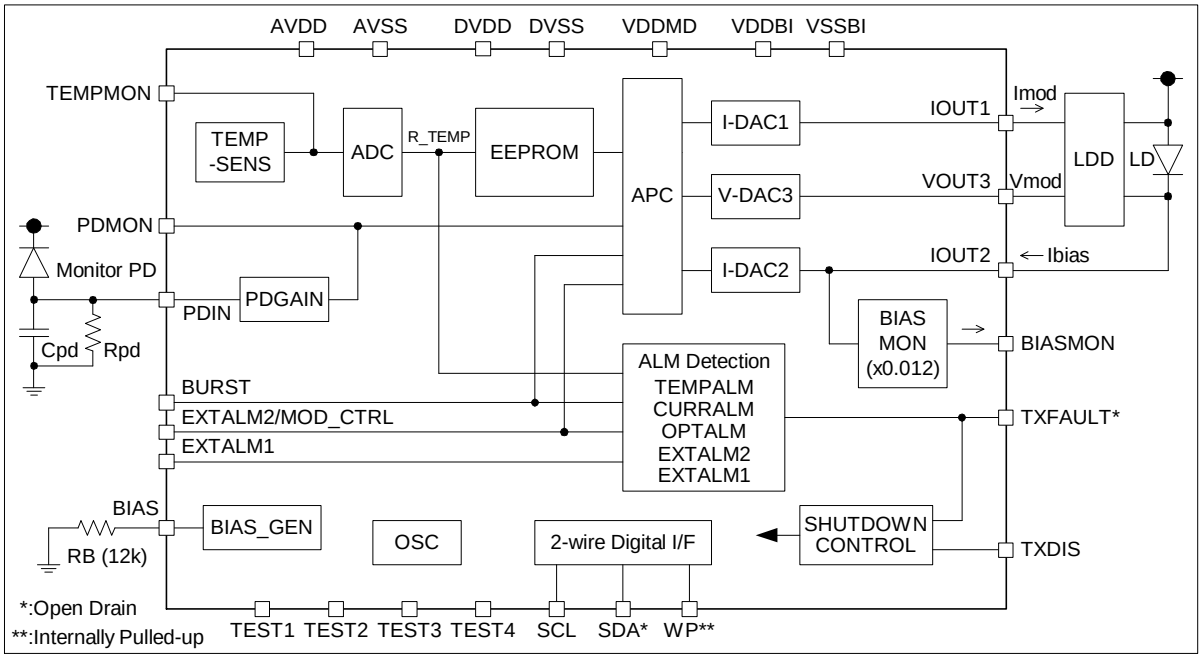
The AK2572 is also applicable to the Burst mode transmission. The device equips a Power leveling function to switch a temperature compensation programming data by either Hardware pin control or Register setting.

The On-chip EEPROM (Non-volatile memory) allows to adjust and to keep the individual setting data for each LD characteristics via 2-wire Digital interface after being assembled into sub-system. As 1k bits User Area is allocated in the EEPROM, which supports the ID field of the SFP specification, a proper operation required for the SFP module is realized by using the TXFAULT function.

ORDERING GUIDE

Product Number	Package Type
AK2572	QFN28 (5.2mm×5.2mm)

BLOCK DIAGRAM



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I. PIN DESCRIPTION

Each symbol at I/O column in the following table means,

PWR : Power (VDD) or VSS, Ai : Analog input, Ao : Analog output,

Di : Digital input, Di_pu : Digital input with pulled-up resistor,

Do : Digital output, Do_od : Digital output (Open drain), Dio_od : Digital input/output (Open drain)

Pin#	Pin Name	Function	I/O	Note
1	TEST1	Input pin for AKM test. Connect it to DVSS for Normal operation.	Di	Connect it to DVSS
2	TEST2	Input pin for AKM test. Connect it to DVSS for Normal operation.	Di	
3	TEST3	Input pin for AKM test. Connect it to DVSS for Normal operation.	Di	
4	DVDD	Power supply for Digital circuit.	PWR	
5	DVSS	Ground for Digital circuit.	PWR	
6	TXFAULT	Alarms such as Optical output decline (OPTALM), Excessive LD current (CURRALM), Exceptional temperature (TEMPALM) and Irregular external signals (EXTALM1 and EXTALM2) can be selected by EEPROM / Register setting as target alarms available on TXFAULT-pin output. When any of the selected alarms (ALM) is detected, TXFAULT-pin becomes "High-Z" output, and it becomes "H" level with a pulled-up resistor connection. This pin is open-drain type and should be connected to DVDD via a 4.7k ~ 10kΩ resistor. With RE_SFP_SET="0" (SFP support mode setting), TXFAULT-pin output is held at "H" level when any of the selected alarms is detected till the shutdown request is released by "H" to "L" transition on TXDIS-pin.	Do_od	Connect it to Pulled-up resistor
7	SDA	Serial data input / output pin for Digital interface. This pin is open-drain type and should be connected to DVDD via a 4.7k ~ 10kΩ resistor.	Dio_od	Connect it to Pulled-up resistor
8	SCL	Serial clock input for Digital interface	Di	Should not be left open
9	BURST	Burst signal input. It is active during "H" input period (valid data period). When this pin is not used, connect it to DVSS.	Di	Should not be left open
10	TXDIS	When this pin is at "H" input, Bias current DAC (I-DAC2) output and Modulation current DAC (I-DAC1 or V-DAC3) output are disabled. Refer to Table 7-1 and Table 7-2. At RE_SFP_SET="0" (SFP support mode setting), a logical sum of TXFAULT output and TXDIS-pin input become a disable request. At RE_SFP_SET="1", TXDIS-pin input becomes a disable request. When this pin is externally pulled-up, use a higher than 4.7kΩ resistor. When this pin is not used, connect it to DVSS.	Di	Should not be left open
11	AVDD	Power supply for Analog circuit.	PWR	
12	AVSS	Ground for Analog circuit.	PWR	
13	PDIN	Monitoring PD (Photo Diode) voltage input. The detected monitor PD current is I to V converted by external resistor and capacitor. Please adjust the cut-off frequency of an LPF to be within 5k ~ 10kHz which is composed of external resistor (Rpd) and capacitor (Cpd). When this pin is not used, it is recommended to connect it to AVSS.	Ai	
14	BIASMON	Bias current monitor. A current multiplied by 0.012 [Typ.] of the I-DAC2 output current is sourced from this pin. When to convert the current to a voltage by an external resistor, select the resistor value such that BIASMON-pin voltage ≦ 1.3 V.	Ao	
15	VSSBI	Ground for I-DAC2.	PWR	

Pin Description (Continued)

Pin#	Pin Name	Function	I/O	Note
16	IOUT2	LD Bias current output (Current-sink type : Maximum sink current =85.0 mA [Typ.]). The current value is set by I-DAC2. Please operate the device under IOUT2-pin voltage≧(VDD−1.7 V) condition. When the voltage on this pin becomes lower, a sink current error becomes larger.	Ao	
17	VSSBI	Ground for I-DAC2	PWR	
18	VDDBI	Power supply for I-DAC2.	PWR	
19	IOUT1	I-DAC1 current output (Current-source type : Maximum sourcing current 10.2 mA [Typ.]). When RE_MODV_SEL = "0", this becomes an LD modulation current output and when RE_MODV_SEL = "1", it is I to V converted and it can be used as an APD control voltage or a reference voltage for LDD (Laser Diode Driver) etc.. Please operate the device under IOUT1-pin voltage≦1.3 V. When the voltage on this pin becomes higher, a sourcing current error becomes larger.	Ao	
20	VDDMD	Power supply for I-DAC1.	PWR	
21	VOUT3	V-DAC3 voltage output pin (Maximum output voltage: 2.2 V [Typ.]). When RE_MODV_SEL="0", this voltage can be used as either an APD control voltage or LDD reference voltage etc.. When RE_MODV_SEL = "1", this outputs an LD modulation current control voltage. Please connect an external RC filter (LPF : R=1kΩ and C=0.01μF are recommended) to this pin.	Ao	Connect it to external RC filter
22	PDMON	PDMON is the Normalized PDIN voltage output pin. Adjust RE_PDGAIN so that PDMON voltage is equal to 1.0 V [typ]. When APC_FB function or OPTALM function is used, RE_PDGAIN adjustment is required.	Ao	
23	TEMPMON	On-chip temperature sensor voltage output.	Ao	
24	BIAS	BIAS resistor connection pin. Connect this pin to AVSS via a 12kΩ±1% resistor.	Ao	Connect it to a resistor
25	EXTALM1	Irregular external signal detect [1] input pin. A polarity of EXTALM1 detection can be selected by RE_EXTALM1_POL. EXTALM1 can be set as a target TXFAULT output alarm by RE_EXTALM1_SET. When this pin is not used, connect it to DVSS.	Di	Should not be left open
26	EXTALM2 / MOD_CTRL	This pin functions as MOD_CTRL input pin when both RE_SFP_SET="1" and RE_PWR_LVL1_SET="1". This pin becomes EXTALM2 input pin when either RE_SFP_SET ="0" or RE_PWR_LVL1_SET="0". When MOD_CTRL-pin function (Power leveling [1] control signal input pin) is selected, Power leveling [1] is executed by a Hardware pin control. In this case, then, EXTALM2-related function is automatically turned off. When EXTALM2-pin function (Irregular external signal detection [2] input pin) is selected, EXTALM2 is set as a target TXFAULT output alarm by RE_EXTALM2_SET, and RE_EXTALM2_POL sets the polarity of EXTALM2 detection. When this pin is not used, connect it to DVSS.	Di	Should not be left open
27	TEST4	Output pin for AKM test. Leave it open for Normal operation.	Do	Open
28	WP	Write protect control pin. This pin is internally pulled-up via a 20kΩ [Typ.] resistor. WP-pin and R_WP_CTRL set the limitation of an accessible EEPROM space via Digital interface. Please refer to Section 9.2 for details.	Di_pu	

Ⅱ. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	VDD	- 0.3	6.0	V	AVDD, DVDD, VDDMD, VDDBI
Ground Level	VSS	0.0	0.0	V	AVSS, DVSS, VSSBI (Base Voltage)
Input Voltage	VIN	VSS－0.3	VDD＋0.3	V	Excluding VDD-pins
Input Current	IIN	- 10	10	mA	Excluding VDD-pins
Storage Temperature	Tstg	- 55	130	℃	

Ⅲ. RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Operating Ambient Temperature	Ta	- 40		+ 85	℃	
Power Supply Voltage	VDD	3.0	3.3	3.5	V	3.3V (-9% / +6%)
	VSS	0.0	0.0	0.0	V	Base Voltage

< Important Notice > Please pay attention not to keep the condition of VDD≦1.5V which makes that the Power On Reset function of AK2572 cannot operate correctly, AK2572 supplies the abnormal LD current and the possibility of damaging LD increases.

Ⅳ. ELECTRICAL CHARACTERISTICS

(1) Current Consumption

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Current Consumption (All VDD-pins)	IDD	－	21	26	mA	[*1], [*2]

[*1] It doesn't include the output current of I-DACs.

[*2] R_DACx＝FFh (x＝1~3), R_DAC1,2_GAIN＝1, R_DAC3_GAIN＝0, PDGAIN＝0dB, PDIN＝1V

(2) EEPROM Characteristics

Item	Min.	Max.	Unit	Condition
EEPROM Write Cycle	1000	－	times	[*]
EEPROM Data Retention Time	10	－	year	Junction temperature Tj＝85℃

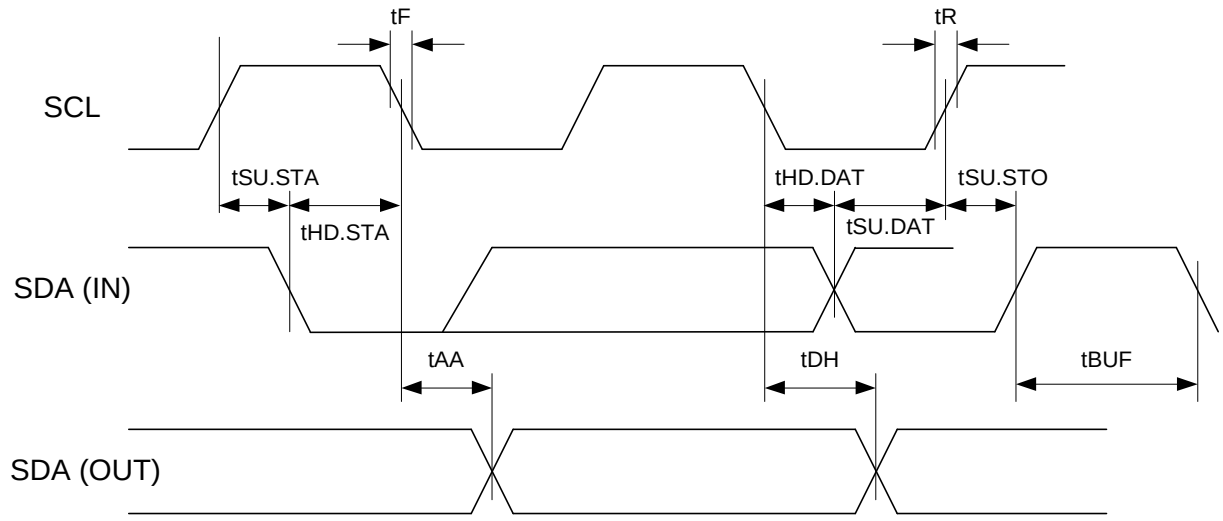
[*] This parameter is characterized and is not 100% tested.

< Important Notice > The adjusted data in AKM factory are stored in advance at address location (Device Address＝A6h, Address＝60h) for the offset voltage of the On-chip temperature sensor. If such excessive temperature stress is to be applied to the AK2572 which exceeds a guaranteed EEPROM data retention conditions (for 10 years at 85℃), it is important to read the pre-determined data in advance and to re-write the same data back into EEPROM after an exposure to the excessive temperature environment. Even if the exposure time is shorter than the retention time, any accelerated temperature stress tests (such as baking) are performed, it is recommended to read the pre-set data first and to re-write it after the test. Access to unused address locations is not functionally guaranteed. Please refer to Section 9.4, "EEPROM Configuration".

(3) Digital Input / Output Pin DC Characteristics

Item	Symbol	Min.	Max.	Unit	Condition
High Level Input Voltage	VIH	2.0		V	
Low Level Input Voltage	VIL		0.8	V	
High Level Output Voltage	VOH	0.9VDD		V	IOH ＝ - 0.2mA
Low Level Output Voltage	VOL		0.4	V	IOL＝1mA (SDA-pin, TXFAULT-pin) IOL＝0.2mA (Excluding SDA, TXFAULT)
Input Leakage Current 1	IL1		10	μA	Excluding WP-pin
Input Leakage Current 2	IL2		350	μA	WP-pin

(4) Digital Input / Output Pin AC Characteristics (Serial Interface)



Symbol	Parameter	Min.	Max.	Unit	Note
tSCL	Clock Frequency, SCL		100	kHz	
tLOW	Clock Pulse Width Low	4.7		μs	
tHIGH	Clock Pulse Width High	4.0		μs	
tI	Noise Suppression Time		100	ns	
tAA	Clock Low to Data Out Valid	0.1	4.5	μs	
tBUF	Time before a New Transmission	4.7		μs	
tHD.STA	Start Hold Time	4.0		μs	
tSU.STA	Start Setup Time	4.7		μs	
tHD.DAT	Data Hold Time	0		μs	
tSU.DAT	Data Setup Time	200		ns	
tR	Input Rise Time		1.0	μs	[*]
tF	Input Fall Time		0.3	μs	[*]
tSU.STO	Stop Setup Time	4.0		μs	
tDH	Data Out Hold Time	100		ns	
tWR	Write Cycle Time		10	ms	

[*] This parameter is characterized and is not 100% tested.

(5) I-DAC1 Characteristics

Item	Condition	Min.	Typ.	Max.	Unit	Note
Resolution			8		bit	Straight Binary
Maximum Output Current 1 (Source)	IOUT1=1.3V	9.4	10.2	11.0	mA	Input Code=FFh RE_DAC1_GAIN=1
Maximum Output Current 2 (Source)	IOUT1=1.3V	0.94	1.02	1.10	mA	Input Code=FFh RE_DAC1_GAIN=0
Current Supply at Shutdown	IOUT1=VSS			10	μA	RE_MODV_SEL=0 TXDIS="H" [*]
1 LSB Current Step 1	IOUT1=1.3V		40.0		μA	RE_DAC1_GAIN=1
1 LSB Current Step 2	IOUT1=1.3V		4.0		μA	RE_DAC1_GAIN=0
DNL	IOUT1=1.3V	-1		+1	LSB	Input Code=10h~FFh
INL	IOUT1=1.3V	-2		+2	LSB	Input Code=10h~FFh

[*] At RE_SFP_SET="0", a logical sum of TXFAULT output and TXDIS-pin input becomes a disable request. Refer to Table 7-1.

(6) I-DAC2 Characteristics

Item	Condition	Min.	Typ.	Max.	Unit	Note
Resolution			8		bit	Straight Binary
Maximum Output Current 1 (Sink)	IOUT2=VDD−1.7V	78.2	85.0	91.8	mA	Input Code=FFh RE_DAC2_GAIN=1
Maximum Output Current 2 (Sink)	IOUT2=VDD−1.7V	39.1	42.5	45.9	mA	Input Code=FFh RE_DAC2_GAIN=0
Current Supply at Shutdown	IOUT2=VDD			100	μA	TXDIS="H" [*]
1 LSB Current Step 1	IOUT2=VDD−1.7V		333		μA	RE_DAC2_GAIN=1
1 LSB Current Step 2	IOUT2=VDD−1.7V		167		μA	RE_DAC2_GAIN=0
DNL	IOUT2=VDD−1.7V	-1		+1	LSB	Input Code=10h~FFh
INL	IOUT2=VDD−1.7V	-2		+2	LSB	Input Code=10h~FFh

[*] At RE_SFP_SET="0", a logical sum of TXFAULT output and TXDIS-pin input becomes a disable request. Refer to Table 7-1.

(7) V-DAC3 Characteristics

Item	Condition	Min.	Typ.	Max.	Unit	Note
Resolution			8		bit	Straight Binary
Maximum Output Voltage 1	10kΩ (to VSS)	1.11	1.20	1.29	V	Input Code=FFh RE_DAC3_GAIN=1
Maximum Output Voltage 2	10kΩ (to VSS)	2.03	2.20	2.37	V	Input Code=FFh RE_DAC3_GAIN=0
Minimum Output Voltage	10kΩ (to VDD)			0.2	V	Input Code=00h
Voltage Supply at Shutdown	10kΩ (to VDD)			0.2	V	RE_MODV_SEL=1 TXDIS="H" [*]
1 LSB Voltage Step 1	10kΩ (to VSS)		4.7		mV	RE_DAC3_GAIN=1
1 LSB Voltage Step 2	10kΩ (to VSS)		8.6		mV	RE_DAC3_GAIN=0
DNL	10kΩ (to VSS)	-1		+1	LSB	Input Code=20h~FFh
INL	10kΩ (to VSS)	-2		+2	LSB	Input Code=20h~FFh

[*] At RE_SFP_SET="0", a logical sum of TXFAULT output and TXDIS-pin input becomes a disable request. Refer to Table 7-1.

(8) Current Monitor (BIASMON)

Item	Condition	Min.	Typ.	Max.	Unit	Note
BIASMON Current	BIASMON=1.3V		0.012		Time	Based on I-DAC2 Input Code=FFh
Maximum Output Current 1 (Source)	BIASMON=1.3V	0.94	1.02	1.10	mA	Input Code=FFh RE_DAC2_GAIN=1
Maximum Output Current 2 (Source)	BIASMON=1.3V	0.47	0.51	0.55	mA	Input Code=FFh RE_DAC2_GAIN=0

(9) PDGAIN

Item	Condition	Min.	Typ.	Max.	Unit	Note
PDIN Input Range	PDMON=1V±10%	0.08		2.5	V	
PDGAIN Gain Error	PDIN→PDMON	- 0.5		+ 0.5	dB	

(10) DAC_APC

Item	Condition	Min.	Typ.	Max.	Unit	Note
Maximum Output Voltage	Test mode, PDMON-pin	1.135	1.195	1.255	V	
Minimum Output Voltage	Test mode, PDMON-pin	0.752	0.792	0.832		
DNL	Test mode, PDMON-pin	- 1		+ 1	LSB	

(11) BIASGEN

Item	Condition	Min.	Typ.	Max.	Unit	Note
BIAS-pin Voltage	12kΩ±1%		1.2		V	

(12) Temperature Sensor

Item	Condition	Min.	Typ.	Max.	Unit	Note
Voltage Slope	TEMPMON-pin Voltage	- 12.14	- 11.56	- 10.98	mV/℃	[*]
Offset Adjustment Target	Ta=35℃		1.215		V	

[*] This parameter is characterized and is not 100% tested.

(13) ADC

Item	Condition	Min.	Typ.	Max.	Unit	Note
Resolution			8		bit	Straight Binary
Maximum Input Voltage		2.09	2.20	2.31	V	±5%
Minimum Input Voltage			0		mV	
DNL		- 1		+ 1	LSB	
INL		- 2		+ 2	LSB	

(14) Power On Reset

Item	Condition	Min.	Typ.	Max.	Unit	Note
Detect Voltage		2.3	2.5	2.7	V	

(15) On-chip Oscillator

Item	Condition	Min.	Typ.	Max.	Unit	Note
Clock Frequency	Test mode		8.192		MHz	

(16) OPTALM

Item	Condition	Min.	Typ.	Max.	Unit	Note
OPTALM Detect Level	1/3 setting, PDGAIN=0dB	1/3.2	1/3	1/2.8	Time	
	1/4 setting, PDGAIN=0dB	1/4.3	1/4	1/3.7	Time	
	1/6 setting, PDGAIN=0dB	1/6.4	1/6	1/5.6	Time	
	1/7 setting, PDGAIN=0dB	1/7.5	1/7	1/6.5	Time	

V. PACKAGE INFORMATION

(1) Package Type : 28 pin - QFN

(2) Marking Information :

a) PIN#1 Indication : ○

b) Marking Code : AK2572

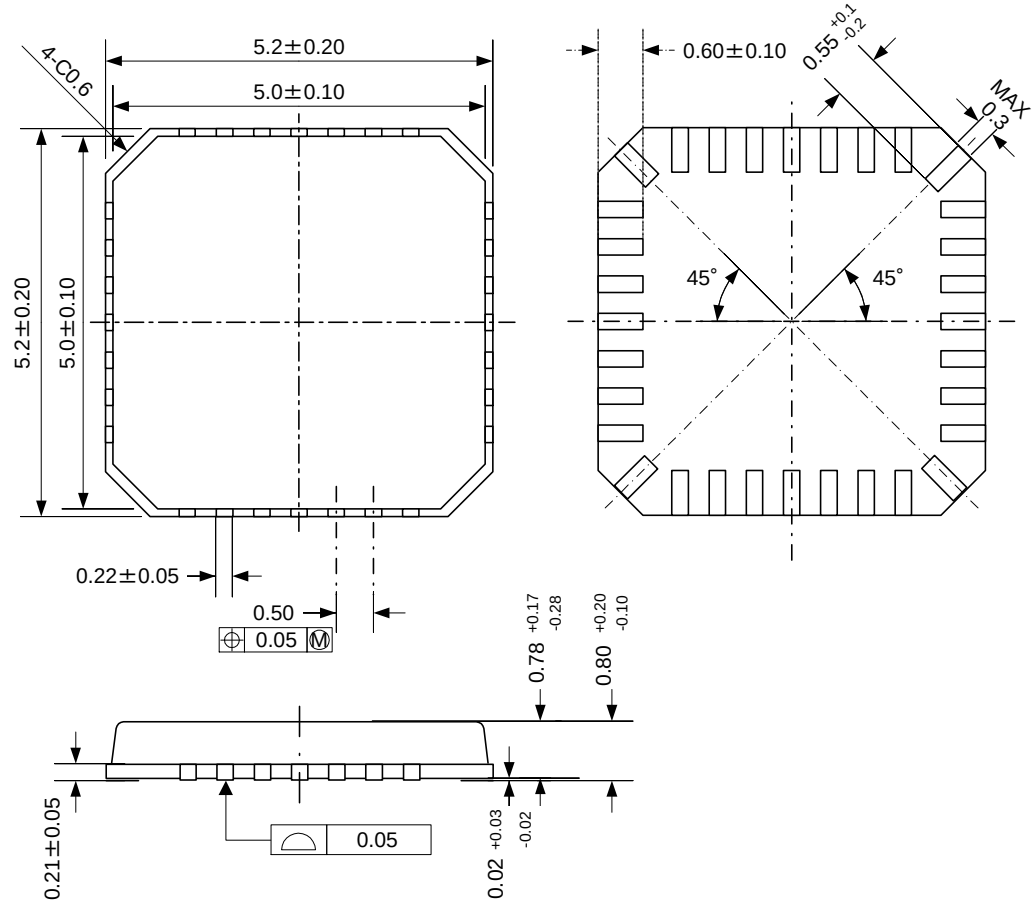
c) Date Code : YWWX (4 Digit)

Y : Year

WW : Week (1 ~ 52)

X : Manufacturing Identification

(3) Package Outline Dimension



VI. CIRCUIT DESCRIPTION

1. Operational Description Notation

In order to distinguish various pre-set parameter sources from EEPROM, Registers or Device pins," Identifier – Main name " notation is used in the AK2572 circuit description as shown in Table 1-1. For ease of operational description, internal signals are sometimes defined which are all expressed in small letters.

Table 1-1 Definition of Terms

	Identifier	Main name	Remark	Example
Register	R_	REGISTER name (All Capital)	Indicating Register	R_DAC2
EEPROM	E_	EEPROM name (All Capital)	Indicating EEPROM	E_BIAS_TC
Either or Both Register or/and EEPROM	RE_	REGISTER name EEPROM name (All Capital)	Indicating either or both Register or/and EEPROM	RE_DAC3_GAIN
BLOCK		BLOCK name (All Capital)		I-DAC1
Internal node		signal name (All small letter)		vpd

Identification words are assigned to the name of Register / EEPROM as shown in Table 1-2 so that each function can be easily assumed by each name.

Table 1-2 Identification Word Classification

Classification	Suffix	Contents	Example
Identification suffix	_SET	Functional setting	RE_APC_FF_SET
	_SEL	Functional selection	E _MODV_SEL
	_TC	Temperature compensation value	E_MOD_TC
	_WIN	Window width setting by ALM set	RE_TEMP_WIN
	_TRGT	Target value	RE_APC_TRGT
Functional identification word	APC	APC related, common for I-DAC1, I-DAC2 and V-DAC3	RE_APC_FF_SET
	DAC	I-DAC, V-DAC related	E_DAC_SET
	BIAS	Bias current (I-DAC2) related	R_BIAS_FF
	MOD	MOD current (I-DAC1, V-DAC3) related	E_MOD_TC
	EXTRA	EXTRA DAC (DAC not set to MOD) related	R_EXTRA
	TEMP	Temperature sensor related	R_TEMP
	PWR	Power leveling function related	R_PWR_SEL
	ALM	Alarm related	R_TEMPALM_SET
	FF	FeedForward function	RE_APC_FF_SET
	FB	FeedBack function	RE_APC_FB_SET
	FBRT	FB dividing	R_MOD_FBRT
	TIMER	Timer related	R_TIMER_OPTALM
	GAIN	Gain adjust	E_DAC1_GAIN
	BURST	Burst mode support function related	E_BURST_ALM
	ST	Status signals	R_TXFLT_ST
	POL	Signal polarity	E_EXTALM1_POL

< Note > Numeric values in the circuit description of the AK2572 are expressed in Binary, Decimal or Hexadecimal. In order to identify the differences, setting values in Hexadecimal are expressed with a small character "h" suffix.

2. Operation Setting

The AK2572 can operate following functions as shown in Table 2-1 by EEPROM / Register setting. For further details, please refer to the circuit description at the next page and thereafter.

Table 2-1 AK2572 Operation Setting

	Set-up				Related setting
RE_BURST_SET	0		1		
RE_SFP_SET [*3]	0	1	1		
RE_PWR_LVL1_SET [*3]	0		0	1	
RE_PWR_LVL2_SET	0		1	0	
RE_APC_FF_SET	00 ~ 11 (0 ~ 3)		11 (3)		
RE_APC_FB_SET	00 ~ 11 (0 ~ 3)		0		
RE_OPTALM_SET	0 / 1		0		
RE_CURRALM_SET	0 / 1		0		
Continuous mode	○		×		
Burst mode	×		○		
SFP_MSA support	○	×	×		
Shutdown request	Logical sum (ORed) of TXFAULT and TXDIS	TXDIS	TXDIS		
Power leveling [1]	×		×	○	MOD_CTRL-pin E_MOD_TC[1] E_MOD_TC[2]
EXTALM2 / MOD_CTRL-pin	EXTALM2		EXTALM2	MOD _CTRL	
Power leveling [2]	×		○	×	RE_PWR_SEL E_BIAS_TC[0]~[3] E_MOD_TC[0]~[3]
APC_FF function	□ [*1]		○ [*2]		
APC_FB function	□ [*1]		× [*2]		
OPTALM	□ [*1]		× [*2]		RE_OPTALM RE_TIMER_OPTALM
CURRALM	□ [*1]		× [*2]		E_CURRALM_BIAS_TC E_CURRALM_MOD_TC

[*1] These functions are determined by the corresponding EEPROM / Register setting. Therefore the operations of "□" depend on the user's setting.

[*2] In Burst mode setting (RE_BURST_SET="1", RE_SFP_SET="1"), it is assumed that only APC_FF function is used and no APC_FB function is used (Monitor PD, CURRALM and OPTALM are not used).

[*3] Setting of RE_SFP_SET="0" and R_PWR_LVL1_SET="1" is prohibited.

3. I-DAC, V-DAC Functional Part

The AK2572 equips Current source type I-DAC1 (Max. sourcing current＝10.2 mA [Typ.]) and Voltage output type V-DAC3 (Max. output voltage＝2.2 V [Typ.]) for the LD modulation current setting, and Current sink type I-DAC2 (Max. sink current＝85.0 mA [Typ.]) for the bias current setting. Selection of enable / disable each DAC is set by RE_DAC_SET. Output current of I-DAC1 (Max. value＝10.2 mA / 1.02 mA [Typ.]) and I-DAC2 (Max. value＝85.0 mA / 42.5 mA [Typ.]), and output voltage of V-DAC3 (Max. value＝2.2 V / 1.2 V [Typ.]) can be switched by gain setting. This gain switching allows to lower current consumption and to improve the accuracy per 1 LSB. In Tables 3-1 ~ 3-3, the characteristics of I-DAC2, I-DAC1 and V-DAC3 are shown.
I-DAC2 directly sets the LD bias current. A current multiplied by a factor of 0.012 [Typ.] of I-DAC2 set value is output (Current source) on BIASMON-pin.

Table 3-1 I-DAC2 characteristics (I-DAC2 is set "Enabled" / "Disabled" by RE_DAC_SET [1]＝"1" / "0")

RE_DAC2_GAIN	Gain	Max. output current (Code＝FFh)[Typ]	Range [Typ]	Current/step [Typ]
1	1	85.0 mA	0 ~ 85.0 mA	333 μA
0	1/2	42.5 mA	0 ~ 42.5 mA	167 μA

[Note] I-DAC2 characteristics : Resolution＝8 bits, DNL＝±1 LSB (DAC code＝10h ~ FFh)
Output current variation at Maximum DAC code (FFh)＝Typ.±8 %

Temperature compensation data (Retained in EEPROM), which are set for I-DAC1 and V-DAC3, can be selected by RE_MODV_SEL setting as shown in Table 3-4.
When E_MOD_TC (128 address locations) is assigned as the setting data, I-DAC1(RE_MODV_SEL＝"0") generates a reference current of the modulation current to external Laser Diode Driver (LDD), and V-DAC3 (RE_MODV_SEL＝"1") generates a reference voltage of the Modulation current to external LDD. A voltage driver type LDD can also be adopted by converting an I-DAC1 output current to a voltage by external resistors or by using V-DAC3 output voltage. When E_EXTRA_TC (32 address locations) is assigned as the setting data, I-DAC1 output (RE_MODV_SEL＝"1") or V-DAC3 output (RE_MODV_SEL＝"0") can be used as APD control voltage or LDD reference voltage etc.. When temperature compensation by E_EXTRA_TC is not required, same data should be written at all address locations.

Table 3-2 I-DAC1 characteristics (I-DAC1 is set "Enabled" / "Disabled" by RE_DAC_SET [0]＝"1" / "0")

RE_DAC1_GAIN	Gain	Max. output current (Code＝FFh)[Typ]	Range [Typ]	Current / step [Typ]
1	1	10 .2 mA	0 ~ 10 .2 mA	40 μA
0	1/10	1.02 mA	0 ~ 1.02 mA	4 μA

[Note] I-DAC1 characteristics : Resolution＝8 bits, DNL＝±1 LSB (DAC code＝10h ~ FFh)
Output current variation at Maximum DAC code (FFh)＝Typ.±8 %

Table 3-3 V-DAC3 characteristics (V-DAC3 is set "Enabled" / "Disabled" by RE_DAC_SET [2]＝"1" / "0")

RE_DAC3_GAIN	Gain	Max. output voltage (Code＝FFh)[Typ]	Range [Typ]	Voltage / step [Typ]
1	1.2 / 2.2	1.2 V	0 ~ 1.2 V	4.7 mV
0	1	2.2 V	0 ~ 2.2 V	8.6 mV

[Note] V-DAC3characteristics : Resolution＝8 bits, DNL＝±1 LSB (DAC code＝20h ~ FFh)
Output voltage variation at Maximum DAC code (FFh)＝Typ.±8 %

Table 3-4 RE_MODV_SEL setting

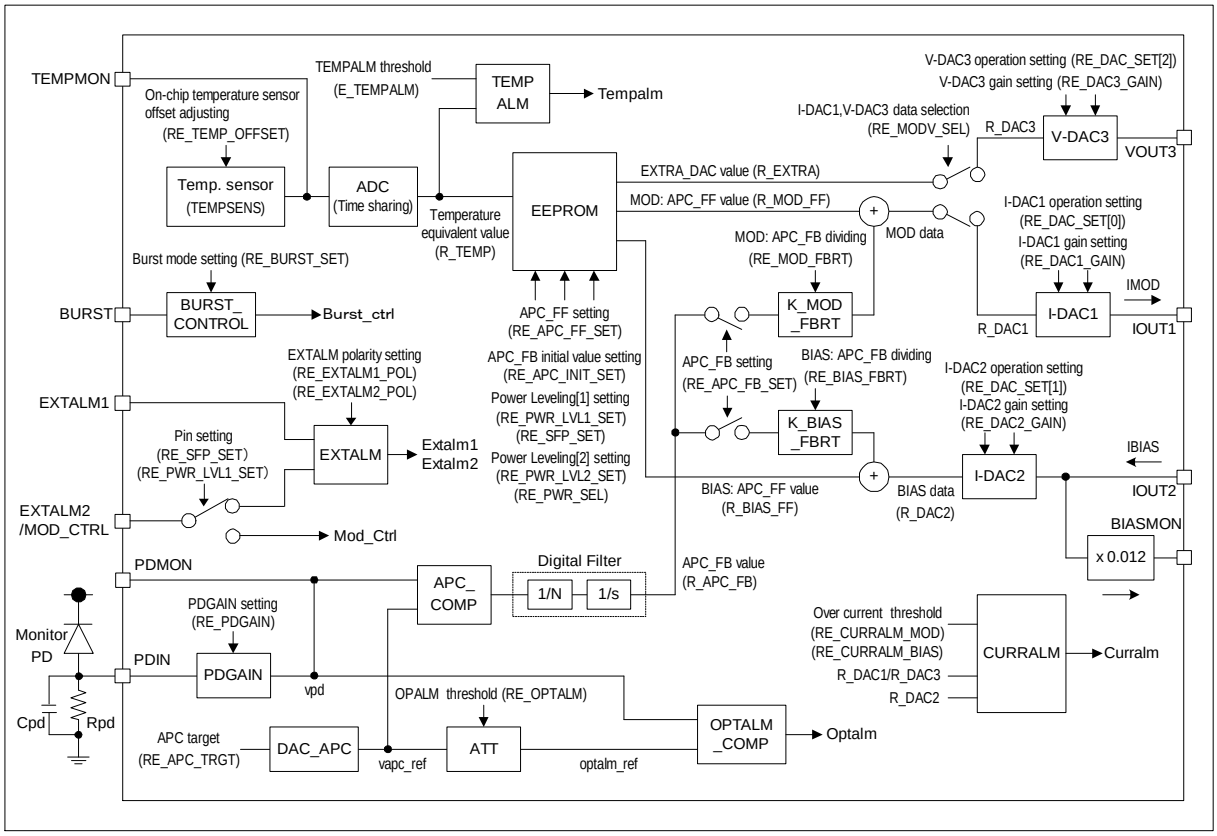
RE_MODV_SEL	I-DAC1	V-DAC3
0	E_MOD_TC	E_EXTRA_TC
1	E_EXTRA_TC	E_MOD_TC

[Note] Although E_MOD_TC has 128 address locations and E_EXTRA_TC has 32 address locations, temperature resolution of each temperature compensation data is 0.75 ℃ [typ.] because of the temperature compensation data is derived from a linear interpolation method (Refer to Section 4.1).

4. APC Functional Part

Circuit configuration of the APC part is shown in Figure 4-1. The AK2572 is formed with APC_FF function which sets the programmed current with corresponding to the detected temperature by On-chip temperature sensor and APC_FB function which controls with feedback function to keep the monitoring photo diode current constant. By properly combining APC_FF and APC_FB functions together by EEPROM / Register setting, a proper LD Bias current / Modulation current can be generated.

Figure 4-1 APC Circuit Block Diagram



4. 1 APC_FF Function

APC_FF functional block diagram is shown in Figure 4-2. Output voltage of On-chip temperature sensor, which responds to the detected temperature, is A-to-D converted (8 bits) in every temperature detection cycle (64 msec [Typ.]). The resulting data (R_TEMP) is used as an EEPROM address and the data (8 bits) retained in EEPROM at that address location is read out. The read out data is set to DAC and by supplying a proper current to LD in response to temperature characteristics of each LD, APC_FF function is realized as in the procedure above. Namely, the EEPROM address corresponds to temperature and the data corresponds to the bias current and the modulation current at that temperature.

Although allocated EEPROM space for APC_FF is 7 bits (128 address locations), it is extended to 8 bits equivalent data (256 address locations) by utilizing a linear interpolation of the current programming data as shown in the following equation.

< Linear interpolation of E_BIAS_TC and E_MOD_TC >

Given that the detected temperature data are R_TEMP[7:0]=z=2x, 2x+1, R_TEMP[7:1]=x, and the temperature compensated data retained in EEPROM are E_BIAS_TC(x), E_MOD_TC(x), and the data derived from linear interpolation are R_BIAS_FF(z), R_MOD_FF(z) respectively,

$$R\_BIAS\_FF(z) = E\_BIAS\_TC(x-1) + \{E\_BIAS\_TC(x) - E\_BIAS\_TC(x-1)\} \times R\_TEMP[0]/2$$

$$R\_MOD\_FF(z) = E\_MOD\_TC(x-1) + \{E\_MOD\_TC(x) - E\_MOD\_TC(x-1)\} \times R\_TEMP[0]/2$$

But at x=0 (R_TEMP[7:0]=z=0, 1), E_BIAS_TC(x)=E_BIAS_TC(x−1)=E_BIAS_TC(0)

E_MOD_TC(x)=E_MOD_TC(x−1)=E_MOD_TC(0)

< Linear interpolation of E_EXTRA_TC >

Given that the detected temperature data are R_TEMP[7:0]=z=8y, 8y+1, ···, 8y+7, R_TEMP[7:3]=y, and the temperature compensated data retained in EEPROM is E_EXTRA_TC(y), and data calculated by linear interpolation is R_EXTRA(z) (DAC loading E_EXTRA_TC data is selected by RE_MODV_SEL),

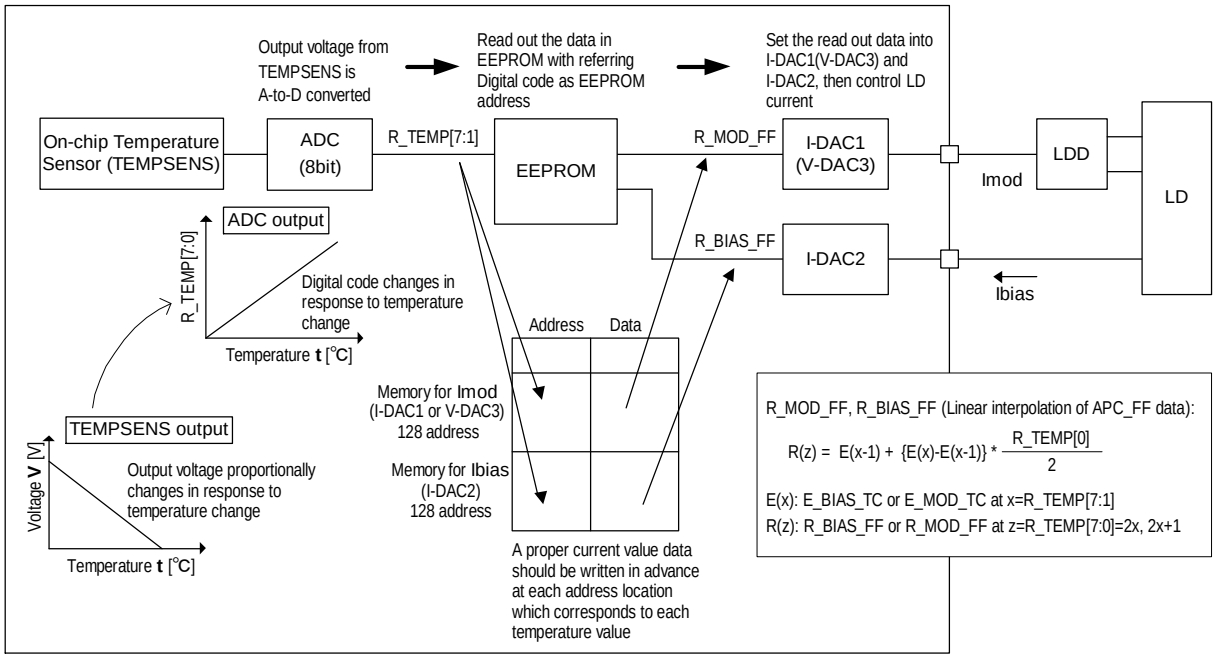
$$R\_EXTRA(z) = E\_EXTRA\_TC(y-1) + \{E\_EXTRA\_TC(y) - E\_EXTRA\_TC(y-1)\} \times R\_TEMP[2:0] / 8$$

But at y=0 (R_TEMP[7:0]=z=0 ~ 7), E_EXTRA_TC(y)=E_EXTRA_TC(y−1)=E_EXTRA_TC(0)

In order to keep the optical power of LD constant by APC_FF method, regardless of environmental temperature changes, it is necessary to write and store the data of Bias current and Modulation current at each in the temperature-corresponding EEPROM address when to adjust each LD module. In normal operation, On-chip oscillator for temperature compensation of the current to drive LD modules automatically executes the temperature detection and the current setting.

Those temperature compensated data for Bias current, Modulation current and EXTRA_DAC which are all derived from the linear interpolation, have approximately 0.75 ℃ resolution and can automatically adjust LD current and reference voltage for external circuit in approximately 0.75 ℃ step. The On-chip temperature sensor is designed to cover the temperature range from - 40 ℃ ~ +115 ℃ under the ADC operating voltage range (0 ~ 2.2 V [Typ.]). As to the relation between temperature sensor and ADC code, please refer to Section “4.4 On-chip Temperature Sensor Characteristics“.

Figure 4-2 APC_FF Functional Block Diagram



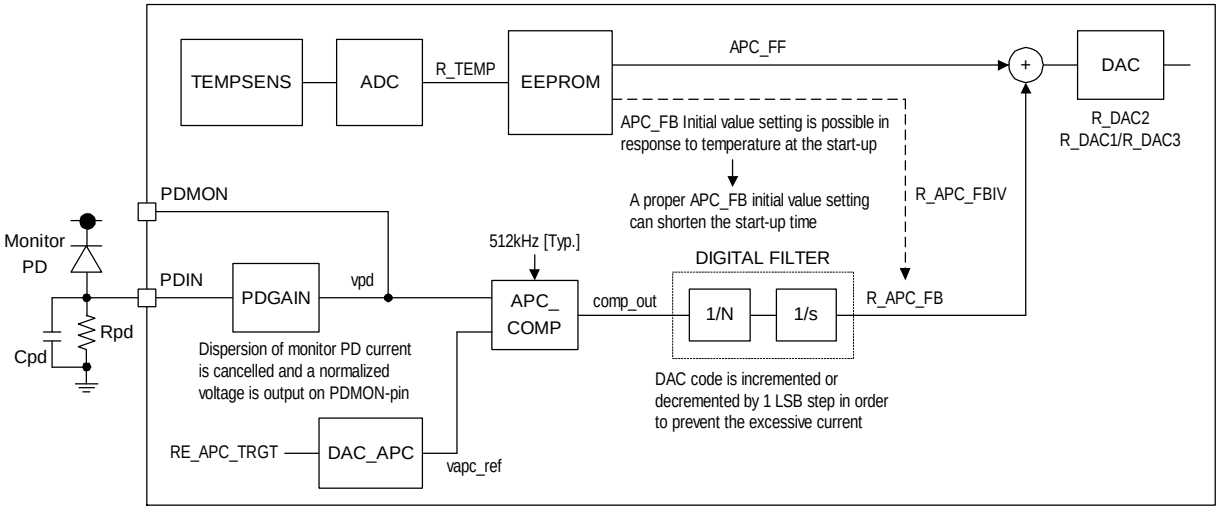
4.2 APC_FB Function

APC_FB functional block diagram is shown in Figure 4-3.

In APC_FB block, an amplified PDIN voltage by gain value (vpd) and DAC_APC output voltage (vapc_ref) are compared at APC_COMP, and the feedback current (R_APC_FB) is calculated at digital filter so that vpd and vapc_ref are equal. The cut-off frequency (fpd), which is fixed by Rpd and Cpd, should be set as follows:

5 kHz＜fpd＜10 kHz

Figure 4-3 APC_FB Functional Block Diagram



4.2.1 APC_FB Circuit Block Diagram

The operation of each block is shown in Table 4-1.

Table 4-1 APC_FB Block Diagram Descriptions

Block	Function	Note
APC_ COMP	Amplified PDIN voltage by gain value (vpd) and APC target value (vapc_ref) are compared and if "vpd＜vapc_ref", UP (increment) request or if "vpd≧vapc_ref", DOWN (decrement) request is output on digital filter. The comparison is made at 512 kHz [Typ.].	
DIGITAL FILTER	From the APC_COMP result, R_APC_FB value is calculated so that vpd and vapc_ref are equal.	
PDGAIN	Amplified PDIN voltage by gain value is output on PDMON-pin. Input range is 0.08 V ~ 2.5V. Adjust the gain so that PDMON output voltage is equal to 1.0V [Typ.]. When to set a normalized voltage lower than 1.0 V, adjust it by utilizing external resistor-divider etc..	
DAC_APC	APC reference voltage (vapc_ref) is output. Output voltage is adjustable by RE_APC_TRGT setting. APC_FB operates such that the amplified PDIN voltage by gain value equals to DAC_APC output.	

4.2.2 Normalization of PD Monitoring Current

A monitor PD current is converted into average voltage by an external resistor and a capacitor and it is fed on PDIN-pin. Input voltage range of PDIN at initial adjustment is listed in Table 4-2.

PDIN voltage is amplified by gain value at PDGAIN block and it is output on PDMON-pin. Adjust PDGAIN so that output voltage on PDMON-pin is 1.0 V [Typ.]. In Table 4-3, adjustable range of RE_PDGAIN is listed. When a lower than 1.0 V [Typ.] is required as a normalized voltage, voltage-divide it by an external resistor-divider etc..

Table 4-2 PDIN Input Condition

Item	Min.	Max.	Note
PDIN input voltage	0.08V	2.5V	

Table 4-3 PDGAIN Setting

RE_PDGAIN	Set-up gain [Typ.]	Note
00 0000 (00h)	23.5 dB	0.5 dB / step
00 0001 (01h)	23.0 dB	
…	…	
11 1110 (3Eh)	- 7.5 dB	
11 1111 (3Fh)	- 8.0 dB	

4.2.3 DAC_APC

DAC_APC outputs APC_FB reference voltage (vapc_ref). vapc_ref is adjusted by RE_APC_TRGT.
The relation of RE_APC_TRGT and vapc_ref is shown in Table 4-4.

Table 4-4 DAC_APC Setting

R_APC_TRGT	DAC_APC output : vapc_ref [Typ.]	Note
0 0000 (00h)	0.792 V	13mV / step
…	…	
0 1111 (0Fh)	0.987 V	
1 0000 (10h)	1.000 V	
1 0001 (11h)	1.013 V	
…	…	
1 1111 (1Fh)	1.195 V	

4.2.4 APC_FB Dividing Function

The AK2572 has a function to divide the R_APC_FB value into both Bias current and Modulation current, which is calculated by APC_FB function. By utilizing this function, the extinction ratio can be kept constant by applying feedback operation on Bias and Modulation currents.
Block diagram in Figure 4-4 and the coefficient factor used for dividing calculation in Table 4-5 are shown.

Figure 4-4 APC Feedback Dividing Block Diagram

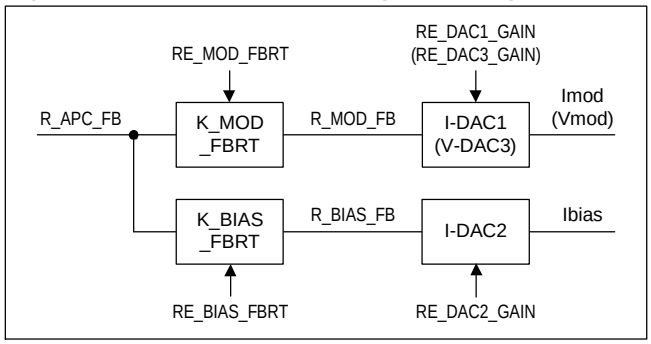


Table 4-5 K_BIAS_FBRT, K_MOD_FBRT

RE_APC_FB_SET	K_BIAS_FBRT	K_MOD_FBRT	Note
00 (0)	0	0	Without Feed Back (FB)
01 (1)	0	1	FB on Modulation current control only
10 (2)	1	0	FB on Bias current control only
11 (3)	R_BIAS_FBRT/128	R_MOD_FBRT/128	FB ratio is divided for both Bias and Modulation currents [*]

[*] R_BIAS_FBRT≦127, R_MOD_FBRT≦127 (Be noted that full range of APC_FB current from I-DACs is limited since the dividing coefficients are mutually multiplied)

4.3 APC Operation Setting

Combination of APC function is set by RE_APC_FF_SET and RE_APC_FB_SET. Setting examples are shown in Table 4-6 and Figures 4-5 ~ 4-13. Handling of the data, which are retained in the temperature compensated Bias data space (E_BIAS_TC) and the temperature compensated Modulation data space (E_MOD_TC), is automatically altered by APC setting. Relation between APC setting and the data retained in EEPROM space is listed in Table 4-7. As to the memory space of E_BIAS_TC and E_MOD_TC, please refer to Table 9-3. Lists of the data for each APC combination are shown in Table 4-8 and 4-9.
RE_APC_FF_SET is configured with 2 bits and it selects the I-DAC for FF (Feed Forward) setting.
RE_APC_FB_SET is configured with 2 bits and it selects the I-DAC for FB (FeedBack) setting.
The upper bit shows the BIAS side and the lower bit shows the MOD (Modulation) side.

Table 4-6 APC Operation Setting Examples

RE_APC _FF_SET	RE_APC _FB_SET	BIAS Current	MOD Current	Note	Figure
01 (1)	10 (2)	FB	FF	Set MOD (Modulation) for FF (Feed Forward) setting. Degraded LD characteristic is compensated by BIAS only. Initial value of BIAS FB (FeedBack) can be programmed in response to a start-up temperature (Set by RE_APC_INIT_SET).	4-5
10 (2)	01 (1)	FF	FB	Set BIAS for FF setting. Degraded LD is compensated by MOD only. Initial value of MOD FB can be programmed in response to a start-up temperature (Set by RE_APC_INIT_SET).	4-6
11 (3)	00 (0)	FF	FF	Set both BIAS and MOD for FF setting. No compensation of degraded LD is made.	4-7
11 (3)	01 (1)	FF	FF+FB	Set both BIAS and MOD for FF setting. Compensation of degraded LD is made by the MOD.	4-8
11 (3)	10 (2)	FF+FB	FF	Set both BIAS and MOD for FF setting. Compensation of degraded LD is made by BIAS.	4-9
00 (0)	11 (3)	FB	FB	Compensation of degraded LD is made in accordance with the dividing coefficient for BIAS and MOD initial value of FB can be programmed in response to a start-up temperature (Set by RE_APC_INIT_SET).	4-10
01 (1)	11 (3)	FB	FF+FB	MOD outputs a current that is sum of the divided FB current and the FF setting current. BIAS outputs a current that is proportional to the divided FB current. Initial value of BIAS FB can be programmed in response to a start-up temperature (Set be RE_APC_INIT_SET).	4-11
10 (2)	11 (3)	FF+FB	FB	BIAS outputs a current that is sum of the divided FB current and the FF setting current. MOD outputs a current that is proportional to the divided FB current. APC_FB initial value setting is prohibited in this setting [*].	4-12
11 (3)	11 (3)	FF+FB	FF+FB	Both in BIAS and MOD, a current that is proportional to the divided FB is added to the FF setting current and compensation of degraded LD is made by the FB current.	4-13

[*] RE_APC_INIT_SET="1" setting is prohibited when RE_APC_FF_SET="10 (2)" and RE_APC_FB_SET ="11 (3)" (BIAS=FF+FB / MOD=FB)

Fig.4-5 Setting Example 1 (BIAS=FB,MOD=FF)

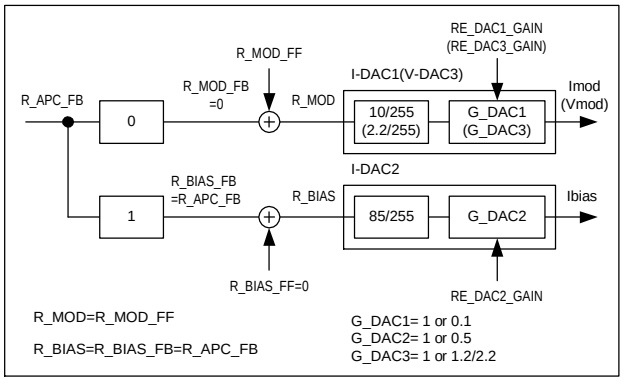


Fig.4-6 Setting Example 2 (BIAS=FF,MOD=FB)

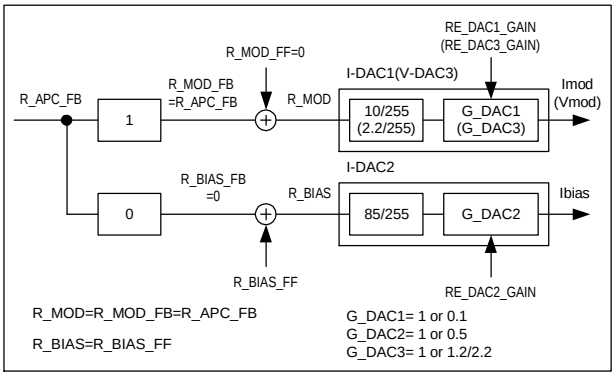


Fig.4-7 Setting Example 3 (BIAS＝FF,MOD＝FF)

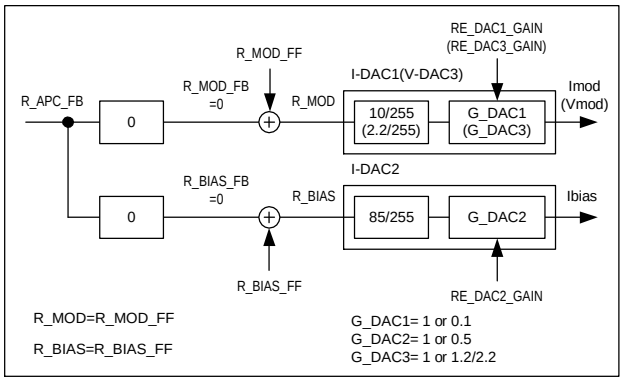


Fig.4-8 Setting Example 4 (BIAS＝FF,MOD＝FF+FB)

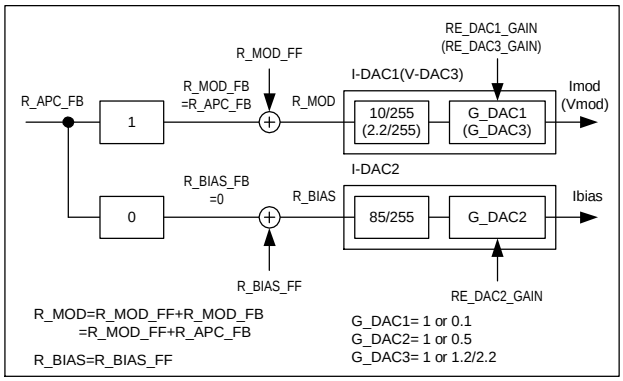


Fig.4-9 Setting Example 5 (BIAS＝FF+FB,MOD＝FF)

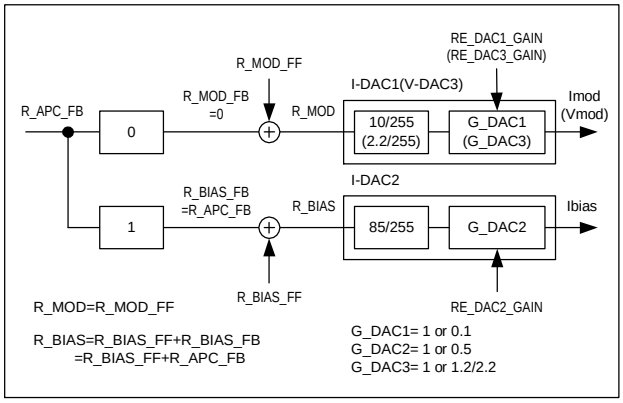


Fig.4-10 Setting Example 6 (BIAS＝FB,MOD＝FB)

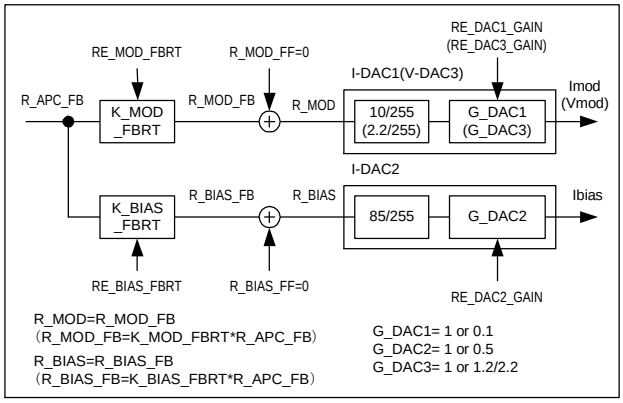


Fig.4-11 Setting Example 7 (BIAS＝FB,MOD＝FF+FB)

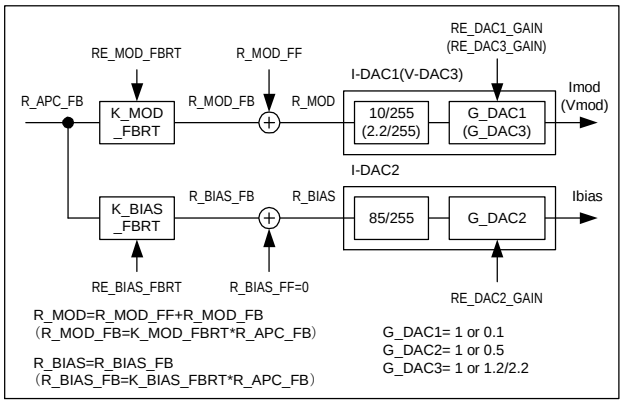


Fig. 4-12 Setting Example 8 (BIAS＝FF+FB,MOD＝FB)

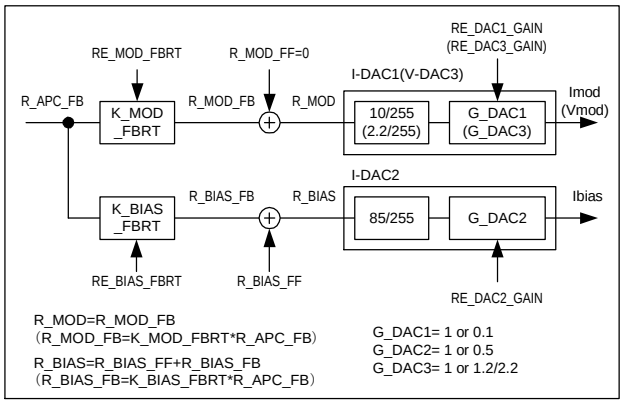


Fig.4-13 Setting Example 9 (BIAS＝FF+FB, MOD＝FF+FB)

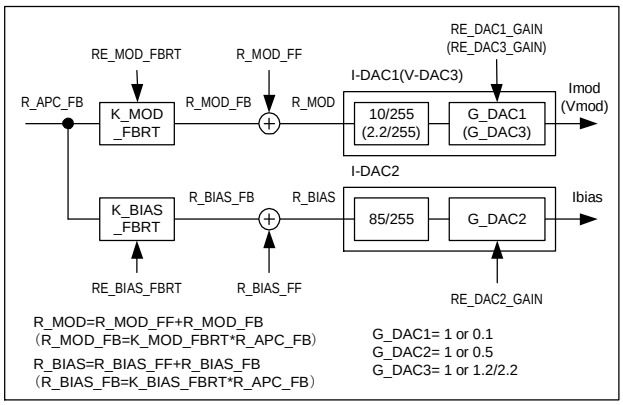


Table 4-7 Relation of APC Operation Setting and Register Retaining Temperature Compensation Data

RE_APC_ FF_SET	RE_APC_ FB_SET	RE_APC_ INIT_SET	E_BIAS_TC [*1] (Temperature compensation Data for I-DAC2)	E_MOD_TC [*1][*2] (Temperature compensation Data for I-DAC1or V-DAC3)
00 (0)	00 (0)	x	–	–
	01 (1)	0	–	–
		1	–	R_APC_FBIV
	10 (2)	0	–	–
		1	R_APC_FBIV	–
	11 (3)	0	–	–
		1	R_APC_FBIV	–
01 (1)	00 (0)	x	–	R_MOD_FF
	01 (1)	0	–	R_MOD_FF
		1	Prohibited	
	10 (2)	0	–	R_MOD_FF
		1	R_APC_FBIV	R_MOD_FF
	11 (3)	0	–	R_MOD_FF
		1	R_APC_FBIV	R_MOD_FF
10 (2)	00 (0)	x	R_BIAS_FF	–
	01 (1)	0	R_BIAS_FF	–
		1	R_BIAS_FF	R_APC_FBIV
	10 (2)	0	R_BIAS_FF	–
		1	Prohibited	
	11 (3)	0	R_BIAS_FF	–
		1	Prohibited	
11 (3)	xx	x	R_BIAS_FF	R_MOD_FF

[*1] As to the EEPROM memory space of E_BIAS_TC, E_MOD_TC, refer to Table 9-3.

[*2] By RE_MODV_SEL setting, DAC (either I-DAC1 or V-DAC3) loading the temperature compensation data retained in E_MOD_TC is selected. Refer to Table 3-4.

[*3] Register content

Register	Content	Note
R_BIAS_FF	Bias current data (APC_FF)	Set to I-DAC2
R_MOD_FF	Modulation current data (APC_FF)	Set to either I-DAC1 or V-DAC3.
R_APC_FBIV	APC_FB initial data.	Added to the APC_FF value after dividing calculation.

Table 4-8 Operation Setting and APC Operation at Self-Operation Mode

RE_APC_FB_SET	RE_APC_FF_SET	RE_APC_INIT_SET	R_BIAS_FF	R_MOD_FF	R_APC_FB	R_APC_FBIV	R_BIAS_FBRT	R_MOD_FBRT	K_BIAS_FBRT	K_MOD_FBRT	(R
00 (0)	00 (0)	x	0	0	0	0	–	–	0	0	
	01 (1)	x	0	E_MOD_TC	0	0	–	–	0	0	
	10 (2)	x	E_BIAS_TC	0	0	0	–	–	0	0	
	11 (3)	x	E_BIAS_TC	E_MOD_TC	0	0	–	–	0	0	
01 (1)	00 (0)	0	0	0	FB	0	–	–	0	1	
		1	0	0	FB	E_MOD_TC	–	–	0	1	
	01 (1)	0	0	E_MOD_TC	FB	0	–	–	0	1	
		1 [*]	–	–	–	–	–	–	–	–	
	10 (2)	0	E_BIAS_TC	0	FB	0	–	–	0	1	
		1	E_BIAS_TC	0	FB	E_MOD_TC	–	–	0	1	
	11 (3)	x	E_BIAS_TC	E_MOD_TC	FB	0	–	–	0	1	
10 (2)	00 (0)	0	0	0	FB	0	–	–	1	0	
		1	0	0	FB	E_BIAS_TC	–	–	1	0	
	01 (1)	0	0	E_MOD_TC	FB	0	–	–	1	0	
		1	0	E_MOD_TC	FB	E_BIAS_TC	–	–	1	0	
	10 (2)	0	E_BIAS_TC	0	FB	0	–	–	1	0	F
		1 [*]	–	–	–	–	–	–	–	–	
	11 (3)	x	E_BIAS_TC	E_MOD_TC	FB	0	–	–	1	0	F
11 (3)	00 (0)	0	0	0	FB	0	E_BIAS_FBRT	E_MOD_FBRT	R_BIAS_FBRT/128	R_MOD_FBRT/128	
		1	0	0	FB	E_BIAS_TC	E_BIAS_FBRT	E_MOD_FBRT	R_BIAS_FBRT/128	R_MOD_FBRT/128	
	01 (1)	0	0	E_MOD_TC	FB	0	E_BIAS_FBRT	E_MOD_FBRT	R_BIAS_FBRT/128	R_MOD_FBRT/128	
		1	0	E_MOD_TC	FB	E_BIAS_TC	E_BIAS_FBRT	E_MOD_FBRT	R_BIAS_FBRT/128	R_MOD_FBRT/128	
	10 (2)	0	E_BIAS_TC	0	FB	0	E_BIAS_FBRT	E_MOD_FBRT	R_BIAS_FBRT/128	R_MOD_FBRT/128	F
		1 [*]	–	–	–	–	–	–	–	–	
	11 (3)	x	E_BIAS_TC	E_MOD_TC	FB	0	E_BIAS_FBRT	E_MOD_FBRT	R_BIAS_FBRT/128	R_MOD_FBRT/128	F

[*] It is prohibited to set <RE_APC_FB_SET="01", RE_APC_FF_SET="01", RE_APC_INIT_SET="1">, <RE_APC_FB_
RE_APC_INIT_SET="1"> or <RE_APC_FB_SET="11", RE_APC_FF_SET="10", RE_APC_INIT_SET="1">.

Table 4-9 Operation Setting and APC Operation at Adjustment Mode

RE_APC _FB_SET	RE_APC _FF_SET	RE_APC_ INIT_SET	R_ BIAS _FF	R_MOD_FF	R_APC_FB	R_APC _FBIV	R_BIAS_ FBRT	R MOD _ FBRT	K_ BIAS _FBRT
00 (0)	x x	x	I/F	I/F	0	0 [*2]	I/F [*1]	I/F [*1]	0
01 (1)	x x	x	I/F	I/F	FB	I/F	I/F [*1]	I/F [*1]	0
10 (2)	x x	x	I/F	I/F	FB	I/F	I/F [*1]	I/F [*1]	1
11 (3)	00 (0)	0	0 [*2]	0 [*2]	FB	0 [*2]	I/F	I/F	R_BIAS_FBRT /128
		1	0 [*2]	0 [*2]	FB	I/F	I/F	I/F	R_BIAS_FBRT /128
	01 (1)	0	0 [*2]	I/F	FB	0 [*2]	I/F	I/F	R_BIAS_FBRT /128
		1	0 [*2]	I/F	FB	I/F	I/F	I/F	R_BIAS_FBRT /128
	10 (2)	0	I/F	0 [*2]	FB	0 [*2]	I/F	I/F	R_BIAS_FBRT /128
		1	I/F	0 [*2]	FB	I/F	I/F	I/F	R_BIAS_FBRT /128
	11 (3)	0	I/F	I/F	FB	0 [*2]	I/F	I/F	R_BIAS_FBRT /128
		1	I/F	I/F	FB	I/F	I/F	I/F	R_BIAS_FBRT /128

"I/F" notation in the table indicates that the register setting can be executed via Digital I/F.

[*1] Setting changes of R_BIAS_FBRT and R_MOD_FBRT are possible via Digital I/F, but APC_FB dividing coefficients K_ not affected.

[*2] Register setting is possible but data is treated as "0".

4.4 On-chip Temperature Sensor (TEMPSENS) Characteristics

Characteristic of the On-chip temperature sensor (TEMPSENS) in Figure 4-14, and the relation of AD code (R_TEMP [7:1] : EEPROM address equivalent) versus Temperature relation in Table 4-10 are shown.

The On-chip temperature sensor characteristic is expressed as :

V [V]＝－0.01156 * t + 1.62 [Typ.]

where temperature t [℃]、and output voltage V [V]. The output voltage of the detected temperature by the temperature sensor has a negative slope characteristic with - 11.56 mV/℃±7% (Reference value by design).

Output voltage from the temperature sensor is A-to-D converted by 8 bits ADC (Max. input voltage＝2.2 V [Typ.]) into the digital code R_TEMP [7:0] and inverted.

7 bits data of the digital code R_TEMP [7:1] is used as EEPROM address, and temperature compensation data for Bias current (E_BIAS_TC) and Modulation current (E_MOD_TC) are read out.

The relation of Temperature and A-to-D converted code is expressed as :

8 bits AD code : R_TEMP[7:0]＝255－int(- 1.334*t +188.3) [Typ.]

7 bits AD code : R_TEMP[7:1]＝127－int(- 0.667*t +94.0) [Typ.]

Be noted that as output voltage from On-chip temperature sensor is A-to-D converted into digital code and inverted, AD code against the detected temperature of On-chip temperature sensor exhibits a positive slope characteristic. Temperature change per each 1 LSB in 8 bits AD code "R_TEMP [7:0]" is +0.75 ℃/LSB [Typ.] and temperature change per each 1 LSB in 7 bits AD code "R_TEMP [7:1]" is +1.5 ℃/LSB [Typ.].

Therefore temperature compensation data for Bias current (E_BIAS_TC) and Modulation current (E_MOD_TC) are written in every 1.5 ℃ increment. However, as the temperature compensation data is derived from a linear interpolation of the detected temperature by the On-chip temperature sensor (refer to Section 4.1), resolution of R_BAIS_FF and R_MOD_FF data to be loaded to DAC is 0.75 ℃. As On-chip temperature sensor detects the chip surface temperature, temperature difference exists between the LD temperature and the detected temperature by the On-chip temperature sensor.

Temperature detect error of the On-chip temperature sensor can be tuned as follows :

(1) Slope calculation at 2 different temperature points :

Read the TEMPSENS output (TEMPMON) or the A-to-D converted code (R_TEMP) at 2 different temperature points and calculate the slope characteristic. It can adjust and correct the characteristics including the error on the slope of the On-chip temperature sensor.

(2) Tuning at a single temperature point :

Read the A-to-D converted code (R_TEMP) while LD adjustment is made, and calculate the AD code at a given temperature, based on the +0.75 ℃ / LSB slope characteristic. It cannot compensate the error of On-chip temperature sensor in this method.

Figure 4-14 On-chip TEMPSENS Characteristics [Typ.]

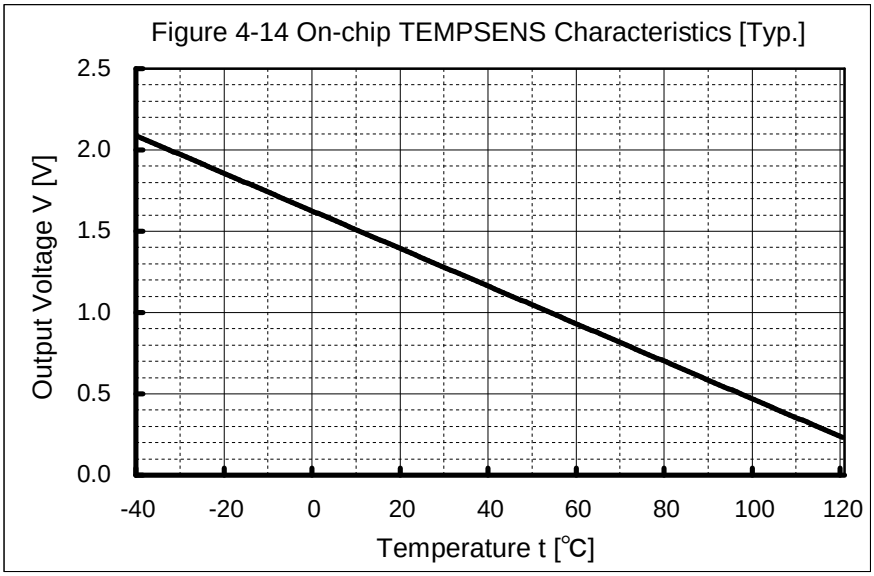


Table 4-10 Relation between R_TEMP[7:1] and detected temperature of the On-chip temperature sensor [Typ.]

R_TEMP [7:1]	Temperature [℃]	R_TEMP [7:1]	Temp. [℃]	R_TEMP [7:1]	Temp. [℃]	R_TEMP [7:1]	Temp. [℃]
0	-50.2	32	-2.2	65	45.7	96	93.7
1	-48.7	33	-0.7	66	47.2	97	95.2
2	-47.2	34	0.8	67	48.7	98	96.7
3	-45.7	35	2.3	68	50.2	99	98.2
4	-44.2	36	3.8	69	51.7	100	99.7
5	-42.7	37	5.3	70	53.2	101	101.2
6	-41.2	38	6.8	71	54.7	102	102.7
7	-39.7	39	8.3	72	56.2	103	104.2
8	-38.2	40	9.8	73	57.7	104	105.7
9	-36.7	41	11.3	74	59.2	105	107.2
10	-35.2	42	12.8	75	60.7	106	108.7
11	-33.7	43	14.3	76	62.2	107	110.2
12	-32.2	44	15.8	77	63.7	108	111.7
13	-30.7	45	17.3	78	65.2	109	113.2
14	-29.2	46	18.8	79	66.7	110	114.7
15	-27.7	47	20.3	80	68.2	111	116.2
16	-26.2	48	21.8	81	69.7	112	117.7
17	-24.7	49	23.3	82	71.2	113	119.2
18	-23.2	50	24.8	83	72.7	114	120.7
19	-21.7	51	26.3	84	74.2	115	122.2
20	-20.2	52	27.7	85	75.7	116	123.7
21	-18.7	53	29.2	86	77.2	117	125.2
22	-17.2	54	30.7	87	78.7	118	126.7
23	-15.7	55	32.2	88	80.2	119	128.2
24	-14.2	56	33.7	89	81.7	120	129.6
25	-12.7	57	35.2	90	83.2	121	131.1
26	-11.2	58	36.7	91	84.7	122	132.6
27	-9.7	59	38.2	92	86.2	123	134.1
28	-8.2	60	39.7	93	87.7	124	135.6
29	-6.7	61	41.2	94	89.2	125	137.1
30	-5.2	62	42.7	95	90.7	126	138.6
31	-3.7	63	44.2	65	92.2	127	140.1

[*] When writing APC_FF data into EEPROM, be noted that AD code data (EEPROM address equivalent where APC_FF data is stored) becomes larger when detected temperature of the On-chip temperature sensor is higher (The relation of detected temperature of the On-chip sensor and output voltage is reversed).

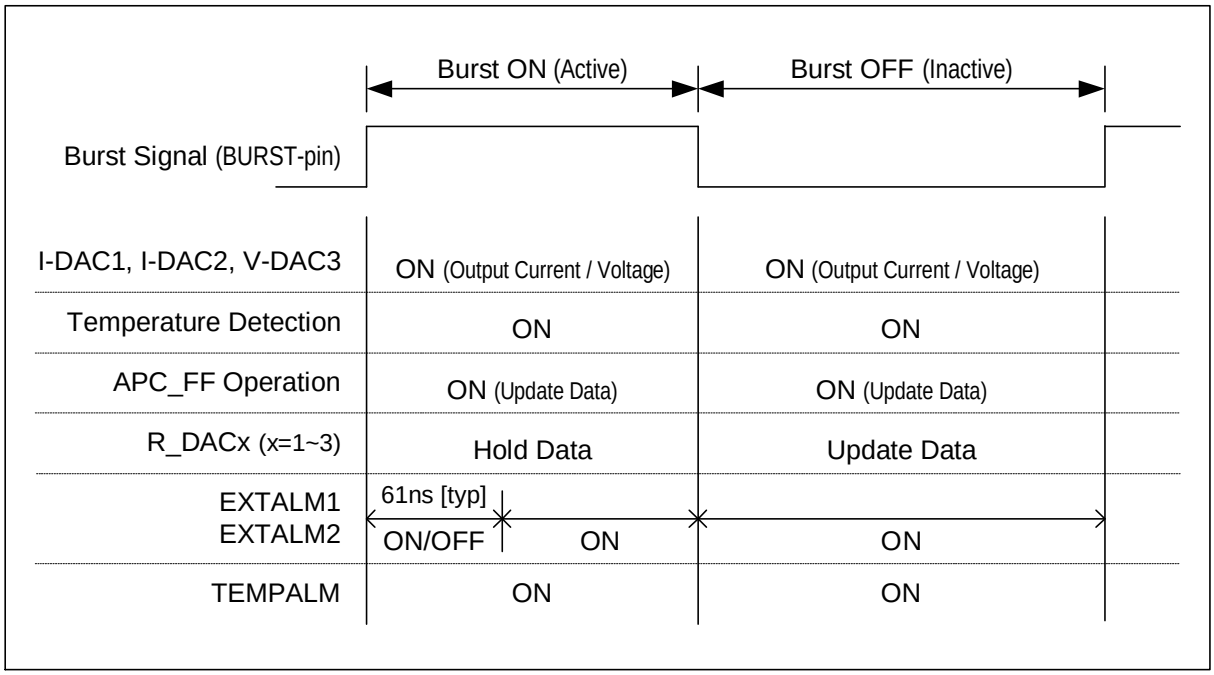
4.5 Current Monitor

A current multiplied by 0.012 factor of the I-DAC2 output current (Sink current) is output as Sourcing current on BIASMON-pin.

5. Burst Mode Operation

The AK2572 is put into Burst mode support operation by setting RE_BURST_SET="1".
When the Burst mode operation is enabled, do not use APC_FB function. Control the LD current by APC_FF function only (RE_APC_FF_SET="3", RE_APC_FB_SET="0"), and OPTALM and CURRALM should not be selected as the target alarm on TXFAULT-pin (RE_OPTALM_SET="0", RE_CURRALM_SET="0").

Figure 5-1 Burst Mode Operation



(1) Alarm mask function

EXTALM1 and EXTALM2 can be masked for 61 ns [Typ.] at the rising edge of Burst signal by RE_BURST_ALM setting. By enabling this masking operation, EXTALM1 and EXTALM2 for TXFAULT-pin output (Logical "OR" function of alarms set by EEPROM / Register) is masked but output to status register R_TXFLT_ST is not masked and ALM detect result is always retained in that register.

(2) APC operation masking function

Updating APC_FF data (R_BIAS_FF, R_MOD_FF) and temperature detection by the On-chip temperature sensor are always executed. DAC setting data (R_DACx [x=1~3]) are updated during the Burst OFF. During the Burst ON, DAC setting data are not updated but the updated data made during the previous Burst OFF period is held.

5. 1 Power Leveling [1]

In Power Leveling [1] mode, the data to be loaded to register (R_MOD_FF) from one of two patterns of the Modulation current temperature compensation data which are retained in EEPROM is selected by Hardware pin control (MOD_CTRL-pin) and it can be used as APC_FF data.
EXTALM2 / MOD_CTRL-pin becomes MOD_CTRL control pin when both RE_PWR_LVL1_SET and RE_SFP_SET are set to "1", and Power Leveling [1] function is available. EEPROM data is set to each DAC by MOD_CTRL-pin as shown in Table 5-1.

Table 5-1 EEPROM Address Space in Power Leveling [1]

RE_MODV_SEL			1		0	
MOD_CTRL-pin			H	L	H	L
EEPROM	Device Address	Address	DAC			
E_MOD_TC [2]	A0h	00h ~ 7Dh [*]	V-DAC3	−	I-DAC1	−
E_MOD_TC [1]	A4h	00h ~ 7Fh	−	V-DAC3	−	I-DAC1
E_BIAS_TC	A4h	80h ~ FFh	I-DAC2	I-DAC2	I-DAC2	I-DAC2
E_EXTRA_TC	A6h	00h ~ 1Fh	I-DAC1	I-DAC1	V-DAC3	V-DAC3

[*] Since Write Protect control register is allocated at "Device Address=A0h / Address=7Eh, 7Fh", E_MOD_TC [2] has 126 address locations. Therefore E_MOD_TC [2] has 2 fewer address locations as compared with E_MOD_TC [1] and E_BIAS_TC. So the linear interpolation of E_MOD_TC [2] is executed as follows :

R_MOD_FF(z)=E_MOD_TC2(x−1)+{E_MOD_TC2(x)−E_MOD_TC2(x−1)}×R_TEMP [0] / 2
when z=R_TEMP [7:0]=0 ~ 5, E_MOD_TC(x)=E_MOD_TC(x−1)=E_MOD_TC(0)

where the detected temperature data is R_TEMP [7:0]=z=2x+5,2x+4, R_TEMP [7:1]=x, E_MOD_TC[2] as E_MOD_TC2(x) and the obtained data by a linear interpolation is R_MOD_FF(z).

5. 2 Power Leveling [2]

In Power Leveling [2] mode, the data to be loaded to register (R_BIAS_FF, R_MOD_FF) can be selected by R_PWR_SEL setting among 4 patterns of Bias current and Modulation current temperature compensation data that are retained in EEPROM.

Power Leveling [2] is enabled by setting RE_PWR_LVL1_SET="0" and RE_PWR_LVL2_SET="1".

When the write protect is released (WP-pin="H" and R_WP_CTRL="0"), R_PWR_SEL [1:0] data at "Device Address=A8h / Address=2Fh" can be altered in Self-Operation Mode.

When Power Leveling [2] is enabled, a linear interpolation of the temperature compensation data is executed by using R_TEMP [7:3], R_TEMP [2:0] and the data in EEPROM as shown in Table 5-2.

R_BIAS_FF(z)=E_BIAS_TCn(y−1)+{E_BIAS_TC n(y)−E_BIAS_TCn(y−1)}×R_TEMP [2:0] / 8
R_MOD_FF(z)=E_MOD_TCn(y−1)+{E_MOD_TCn(y)−E_MOD_TCn(y−1)}×R_TEMP [2:0] / 8
when y=0 (R_TEMP [7:0]=z=0~7), E_BIAS_TCn(y)=E_BIAS_TCn(y−1)=E_BIAS_TCn(0) and E_MOD_TCn(y)=E_MOD_TCn(y−1)=E_MOD_TCn(0).

where the detected temperature data R_TEMP [7:0]=z=8y, 8y+1, ・・・, 8y+7, R_TEMP [7:3]=y, the temperature compensation data retained in EEPROM is E_BIAS_TCn(y), E_MOD_TCn(y), n=0~3 and the obtained data by a linear interpolation is R_BIAS_FF(z), R_MOD_FF(z) respectively.

Table 5-2 EEPROM Address Space in Power Leveling [2]

RE_ PWR_LVL2_SET="0"		
R_TEMP [7:1]	Data	Address
00h ~ 7Fh	E_MOD_TC	00h ~ 7Fh
00h ~ 7Fh	E_BIAS_TC	80h ~ FFh

RE_ PWR_LVL2_SET="1"			
RE_PWR_SEL	R_TEMP [7:3]	Data	Address
0	00h ~ 1Fh	E_MOD0_TC	00h ~ 1Fh
1	00h ~ 1Fh	E_MOD1_TC	20h ~ 3Fh
2	00h ~ 1Fh	E_MOD2_TC	40h ~ 5Fh
3	00h ~ 1Fh	E_MOD3_TC	60h ~ 7Fh
0	00h ~ 1Fh	E_BIAS0_TC	80h ~ 9Fh
1	00h ~ 1Fh	E_BIAS1_TC	A0h ~ BFh
2	00h ~ 1Fh	E_BIAS2_TC	C0h ~ DFh
3	00h ~ 1Fh	E_BIAS3_TC	E0h ~ FFh

6. Alarm Function

In Table 6-1, the outline of the AK2572 Alarm (ALM) functions such as TEMPALM, OPTALM, CURRALM, EXTALM1 and EXTALM2, and TXFAULT output function where alarms to be selected by EEPROM/Register setting are logically OR-ed, are listed.

Table 6-1 ALM Function Outlines

ALM	Condition to output alarm	Detect time [Typ.]	Note
TEMPALM	When detected temperature equivalent value exceeds ALM set value (E_TEMPALM)	64 ms	Temp. sense period=64ms Set by RE_TEMPALM_SET
OPTALM	When monitor PD input voltage becomes lower than ALM set value (RE_OPTALM)	5 μs [*]	Holding APC FB value Set by RE_OPTALM_SET
CURRALM	When a current to be set to DAC exceeds ALM set value (RE_CURRALM_BIAS / MOD)	125 μs	Set by RE_CURRALM_SET
EXTALM1 EXTALM2	When same polarity ALM signal is input on EXTALM1/2-pin as set by RE_EXTALM1/2_POL	1 μs	Set by RE_EXTALM1_SET Set by RE_EXTALM2_SET
TXFAULT	When any of the ALMs is detected as target alarms available on TXFAULT-pin output which are set by EEPROM / Register setting (Refer to note above in this table)	Depend on the detected target alarm	Automatically shutdown when any target alarm is detected and RE_SFP_SET ="0"

[*] The detect time does not include the delay time caused by a time constant of external Rpd and Cpd.

6.1 TEMPALM

TEMPALM is generated when the following relation is established after digitally comparing the A-to-D converted temperature sensor output value (R_TEMP [7:0]) with the ALM set value (R_TEMPALM) :

R_TEMP≧E_TEMPALM

6.2 OPTALM

1/3, 1/4, 1/6 or 1/7 value of the APC target value (apc_ref) can be set as OPTALM set value (optalm_ref) by RE_OPTALM setting. OPTALM detect is done by an analog comparator and it is generated when the following relation is established

vpd＜optalm_ref

6.3 CURRALM

CURRALM is generated when one of the following 3 conditions is met after digitally comparing DAC setting value for Modulation current (R_DAC1 [I-DAC1 set value] or R_DAC3 [V-DAC3 set value]) or DAC setting value for Bias current (R_DAC2 [I-DAC2 set value]) with the CURRALM setting value (R_CURRALM_BIAS, R_CURRALM_MOD):

R_DAC2 (Upper 4 bits)＞R_CURRALM_BIAS

or R_DAC1(Upper 4 bits)＞R_CURRALM_MOD, or R_DAC3(Upper 4 bits)＞R_CURRALM_MOD

Alarm threshold values R_CURRALM_BIAS and R_CURRALM_MOD can be set in accordance with the LD temperature characteristic (Set by approximately every 6 ℃ step with the data in E_CURRALM_BIAS_TC, E_CURRALM_MOD_TC, Refer to Table 9-3).

CURRALM is also generated when either of R_DAC1 (R_DAC3) or R_DAC2 becomes its full code (FFh).

When a shutdown request is made, CURRALM is set to "Inactive" polarity.

6.4 EXTALM1, EXTALM2

When the same polarity ALM signal is input on EXTALM1-pin as set by RE_EXTALM1_POL, EXTALM1 detection is made. On the other hand, when the same polarity ALM signal is input on EXTALM2 / MOD_CTRL-pin as set by RE_EXTALM2_POL, EXTALM2 detection is made if RE_PWR_LVL1_SET＝"0" or RE_SFP_SET＝"0" (EXTALM2 / MOD_CTRL -pin is set to EXTALM2-pin)

When RE_EXTALM1/2_POL＝"0", the ALM detect polarity of "H" at EXTALM1/2-pin is set.

When RE_EXTALM1/2_POL＝"1", the ALM detect polarity of "L" at EXTALM1/2-pin is set.

6. 5 TXFAULT

6.5.1 Target Alarm Setting of TXFAULT Output

As shown in Table 6-2, target Alarms (ALMs) available on TXFAULT output can be selected by EEPROM / Register setting. Logical "OR" function of the selected ALMs becomes TXFAULT output signal.

Table 6-2 Target ALM Setting of TXFAULT Output

Target ALM	Mask setting [*1]	Device Address / Address		Status register (A8h / 19h) [*2]	Note
		EEPROM	Register		
EXTALM2	RE_EXTALM2_SET[5]	A6h / 65h	A8h / 05h	R_TXFLT_ST [3]	[*3]
EXTALM1	RE_EXTALM1_SET[4]			R_TXFLT_ST [2]	
CURRALM	RE_CURRALM _SET[3]			R_TXFLT_ST [1]	
OPTALM	RE_OPTALM _SET[2]			R_TXFLT_ST [0]	
TEMPALM	RE_TEMPALM_SET[7]	A6h / 66h	A8h / 06h	R_TXFLT_ST [4]	

[*1] Logical "OR" function of those ALMs, where corresponding bits are set by "1" in mask setting by EEPROM / Register, becomes TXFAULT output signal.

[*2] When ALM is detected, "1" is written in the corresponding bit of the ALM.status register.

[*3] When RE_PWR_LVL1_SET = "0" or RE_SFP_SET = "0", EXTALM2 / MOD_CTRL-pin is set as EXTALM2 input pin and EXTALM2 function is enabled.

6.5.2 Operation at TXFAULT Detection

Operation at TXFAULT detection differs by RE_SFP_SET setting. Operation at different settings is listed in Table 6-3.

When at RE_SFP_SET="0", any of the ALMs being set by EEPROM / Register is detected, TXFAULT signal is generated and "H" output is held and DAC output is put into shutdown condition. But when a shutdown request is made via TXDIS-pin, a previous TXFAULT output level before the shutdown request is kept and even if any ALM is detected during the shutdown, TXFAULT signal is not output. When the shutdown request is released (transition of "L" to "H") via TXDIS-pin, release of TXFAULT (TXFAULT output is "L") is made. For more details, please refer to section "7. Shutdown Control". DAC output is not shutdown during the Adjustment Mode even if TXFAULT is detected.

When at RE_SFP_SET="1", any of the ALMs being set by EEPROM / Register is detected, TXFAULT signal is generated (TXFAULT output is "H"), when all selected ALMs are cleared, TXFAULT is also cleared (TXFAULT output is "L").

When the shutdown condition is set, CURRALM is forced to "Disabled output" state.

Table 6-3 TXFAULT Operation

RE_SFP_SET	Shutdown request via TXDIS-pin	Logical "OR" of target ALM for TXFAULT	TXFAULT	Operation
0	0	0	0	Normal operation
		1	1 (Hold)	Shutdown
	1	x	Hold the previous TXFAULT level just before shutdown request	Shutdown
1	0	x	Logical "OR" of target ALMs for TXFAULT	Normal operation
	1	x	Logical "OR" of target ALMs for TXFAULT	Shutdown

7. Shutdown Control

7.1 Shutdown Operation

The AK2572 can be put into the shutdown condition by setting TXDIS-pin to "H".
The condition for shutdown in Table 7-1, and operation during shutdown in Table 7-2 are shown.

Table 7-1 Shutdown Condition

TXDIS	RE_SFP_SET	TXFAULT	Operation	Note
0	0	0	Normal operation	
		1	Shutdown	Operation at TXFAULT detection for SFP support
	1	x	Normal operation	
1	x	x	Shutdown	Shutdown request via TXDIS-pin

Table 7-2 Operation during Shutdown

Function	Operation during Shutdown	Note
I-DAC1,2 output	Hi-Z	[*]
V-DAC3 output	0.2 V [Max.]	[*]
APC Feed Forward	Based on the detected temperature, temperature compensation data for I-DAC and V-DAC are updated. But I-DAC output is in Hi-Z state and V-DAC output voltage is 0.2 V [Max.]	
APC Feed Back	During shutdown requested via TXDIS, a value just before the shutdown is held.	
	During shutdown requested by TXFAULT (RE_SFP_SET="0"), a value just before the shutdown is held and it is reset at shutdown release by TXDIS.	
ALM	Normal operation (CURRALM is set to " Disabled output" state)	
TXFAULT	At RE_SFP_SET ="0", a value just before the shutdown is held. At RE_SFP_SET ="1", logical "OR" function of the selected ALMs is output.	

[*] DAC output (I-DAC1 or V-DAC3), which is selected as EXTRA_DAC, is not shutdown.

7.2 Operation at Shutdown Release

Since the AK2572 continues its temperature detection and APC feed forward operation even during the shutdown, current value that is set by Feed Forward function is temperature compensated even if any temperature difference occurs before or after the shutdown.
On the other hand, whether a value just before the shutdown is held or an initial value is set as APC Feed Back data (R_APC_FB) can be selected by RE_TEMP_DET setting. When to hold a value just before the shutdown, a temperature at shutdown release (R_TEMP) and a temperature just before shutdown (to be retained at R_TEMP_STDW) are compared. If the difference is larger than the set value (RE_TEMP_WIN), namely, when the following relation is satisfied, ABS(R_TEMP–R_TEMP_STDW) > RE_TEMP_WIN, a function to set R_APC_FB to initial value is activated so that an excess power emission of LD and a turn-on delay of LD are eliminated. As initialization of R_APC_FB is executed with being based on the detected temperature just before shutdown release, a turn-on operation is accelerated if the initial setting function of APC_FB is selected (RE_APC_INIT_SET="1"). In Table 7-3, R_APC_FB values at shutdown release are listed.

Table 7-3 R_APC_FB Values at Shutdown Release

RE_ SFP_SET	TX- FAULT	RE_ TEMP_DET	Temperature difference	R_APC_FB	Note
0	0	0	x	Initial value	
		1	0	Held value	ABS(TEMP–TEMP_STDW)<TEMP_WIN
			1	Initial value	ABS(TEMP–TEMP_STDW)>TEMP_WIN
	1	x	x	Initial value	Shutdown released by TXDIS
1	x	0	x	Initial value	
		1	0	Held value	ABS(TEMP–TEMP_STDW)<TEMP_WIN
			1	Initial value	ABS(TEMP–TEMP_STDW)>TEMP_WIN

8. Start-Up Setting in SFP Support Mode

8.1 TXFAULT Detection at Power-Up and after Release from Shutdown

8.1.1 OPTALM

In SFP support mode setting (RE_SFP_SET="0"), a mask time can be programmed for TXFAULT detection by OPTALM during the shutdown release so that a time constant delay derived from the external Rpd and Cpd for detection of the averaged monitor-PD current at the turning-on of LD must be taken into consideration. Block diagram in Figure 8-1, and pre-settable mask time relation in Table 8-1 are shown.

In the AK2572, the delay time can be shortened by accelerated start-up setting which is made by initial value setting function of R_APC_FB and so on.

But when OPTALM is selected as one of the TXFAULT target ALMs, and a mask time is set to be shortened, be noted that LD optical power will not reach the expected level within the mask time and it may be shutdown through OPTALM detection to TXFAULT control sequence if initial set value of APC_FF or APC_FB is far off.

Figure 8-1 OPTALM Detection Block Diagram

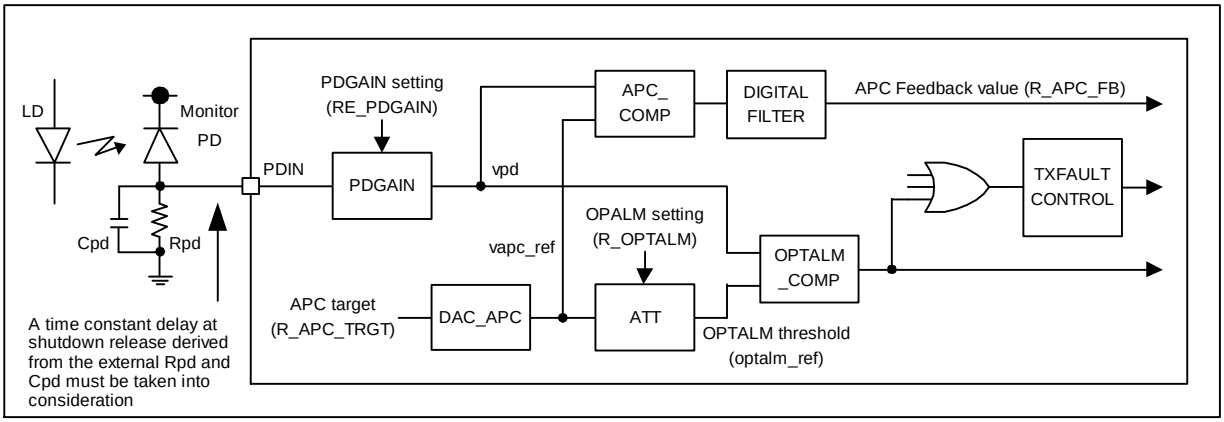


Table 8-1 Time to Valid TXFAULT Detection by OPTALM

RE_ SFP_SET	RE_TIMER _OPTALM	RE_APC_ INIT_SET	RE_APC _FF_SET	Mask time for TXFAULT detection by OPTALM	Note
0	0	x	x	160 ms [Typ.]	
	1	0	00, 01, 10	160 ms [Typ.]	
		x	11	2 ms [Typ.]	Accelerated start-up setting
		1	x	2 ms [Typ.]	Accelerated start-up setting
1	x	x	x	0 ms	Non-support SFP

8.1.2 EXTALM1, EXTALM2

In SFP support mode setting (RE_SFP_SET="0"), a mask time can be set for TXFAULT detection by EXTALM1 and EXTALM2 at the shutdown release.

In Table 8-2, a delay time relation to be set is shown.

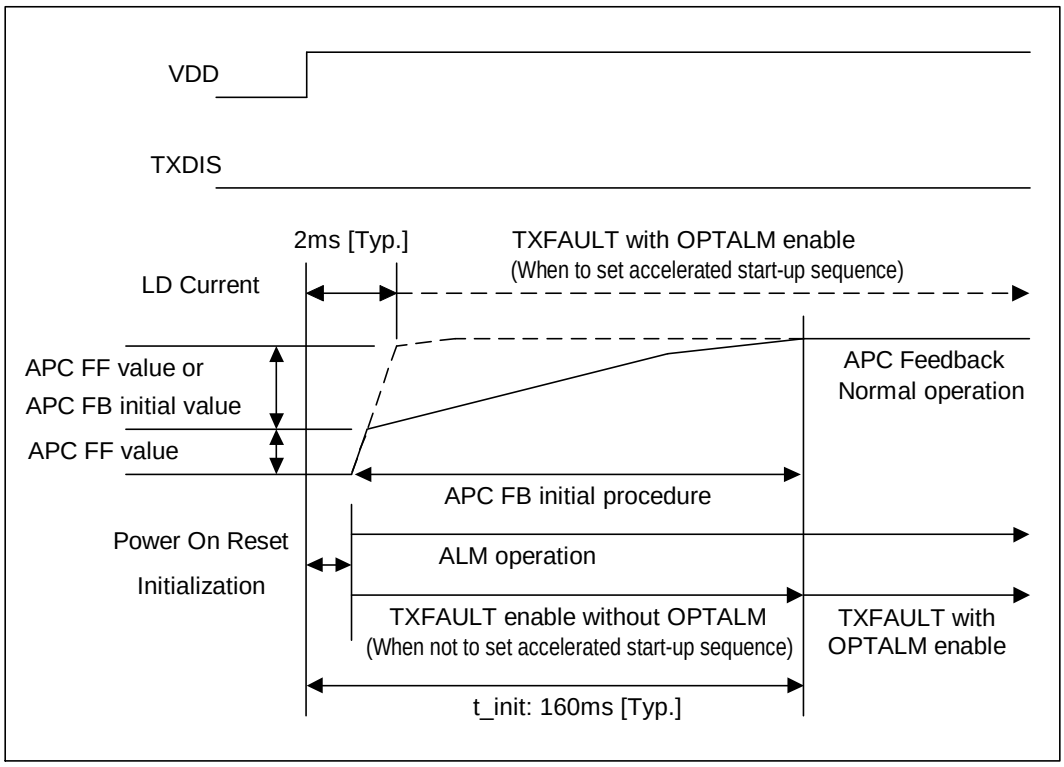
Table 8-2 Time to Valid TXFAULT Detection by EXTALM1, EXTALM2

RE_SFP_SET	RE_TIMER_EXTALM1 RE_TIMER_EXTALM2	Mask time for TXFAULT detection by EXTALM1, EXTALM 2	Note
0	0	0 ms	
	1	2 ms [Typ.]	
1	X	0 ms	Non-support SFP

8.2 At Power-On (at TXDIS="L")

Start-up sequence at power-on (at TXDIS="L") is shown in Figure 8-2.

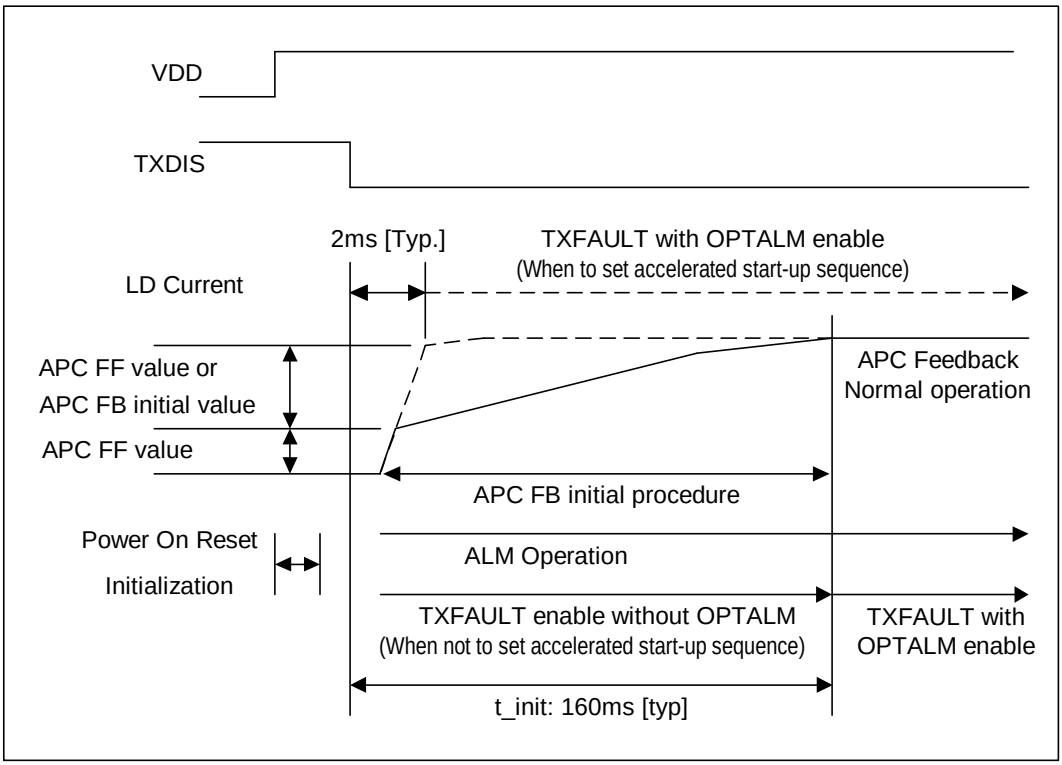
Figure 8-2 Start-up Sequence at Power-on (at TXDIS="L")



8.3 At Power-On (at TXDIS="H")

Start-up sequence at power-on (at TXDIS="H") is shown in Figure 8-3.

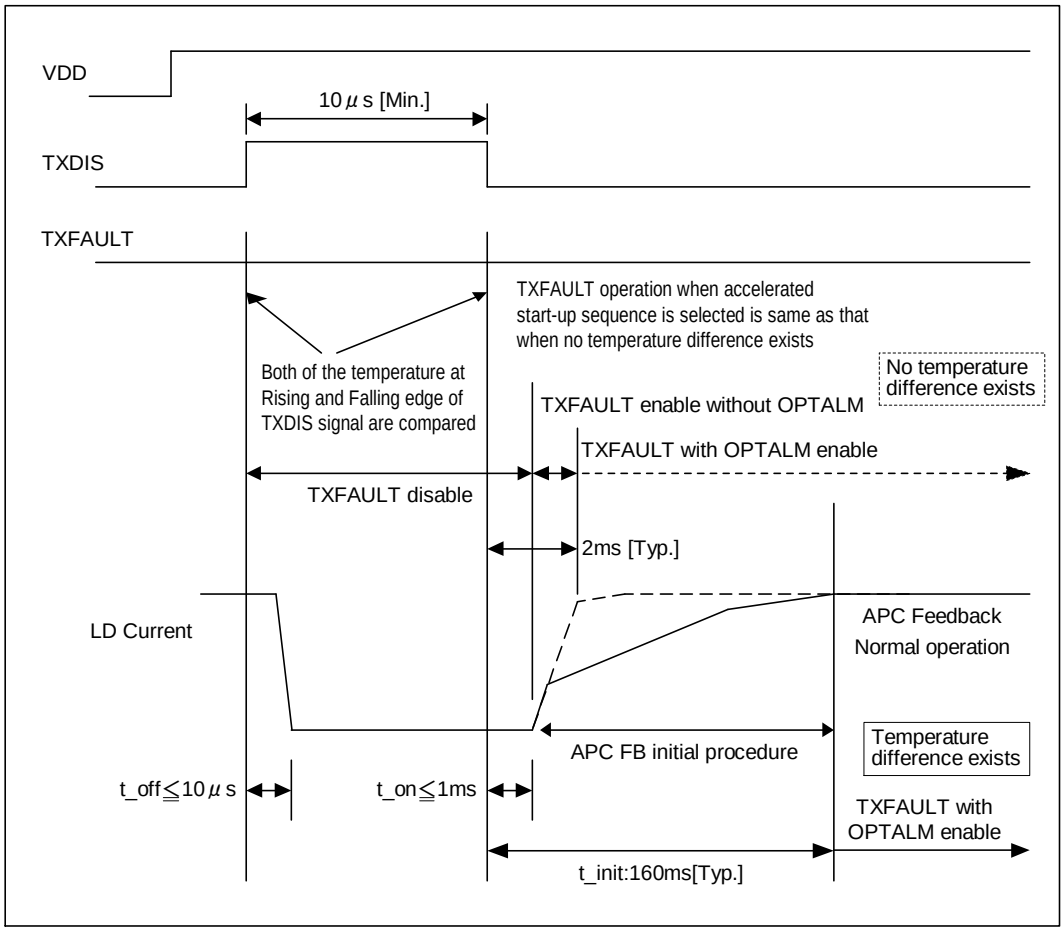
Figure 8-3 Start-up Sequence at Power-on (at TXDIS="H")



8.4 At TXDIS Detection / Release

TXDIS detection / release sequence is shown in Figure 8-4.

Figure 8-4 TXDIS Detection / Release Sequence



8.5 At TXFAULT Detection / Release

TXFAULT detection / release sequences are shown in Figure 8-5 and Figure 8-6.

Figure 8-5 TXFAULT Detection / Release Sequence (When FAULT is released by TXDIS reset)

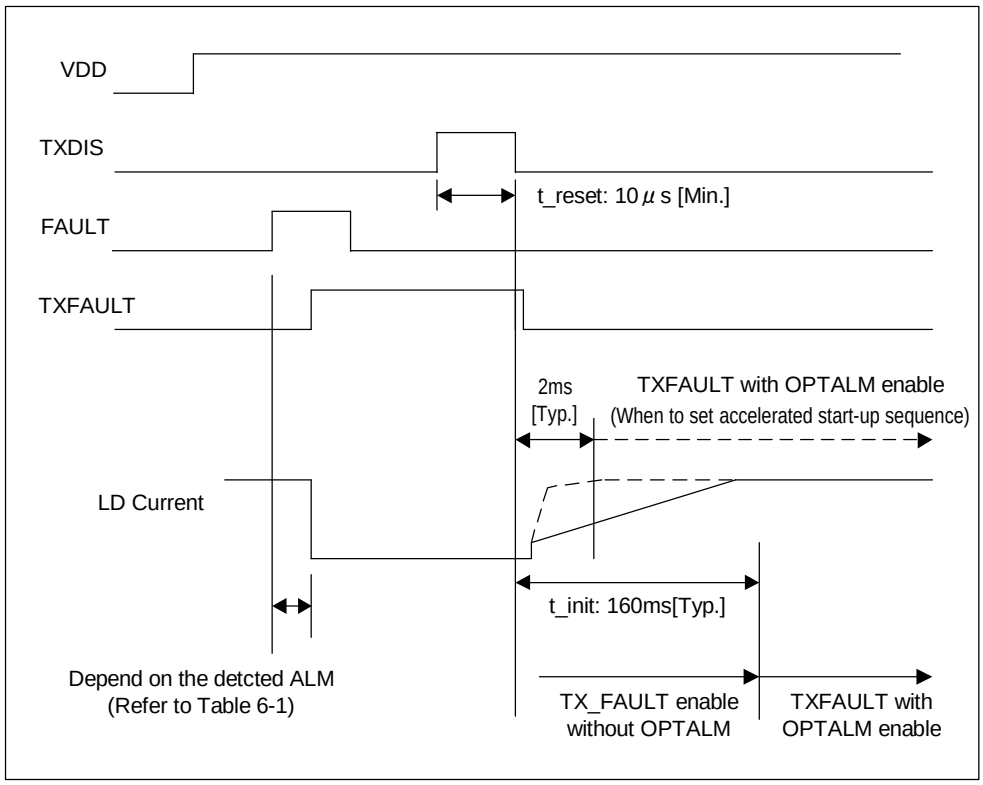
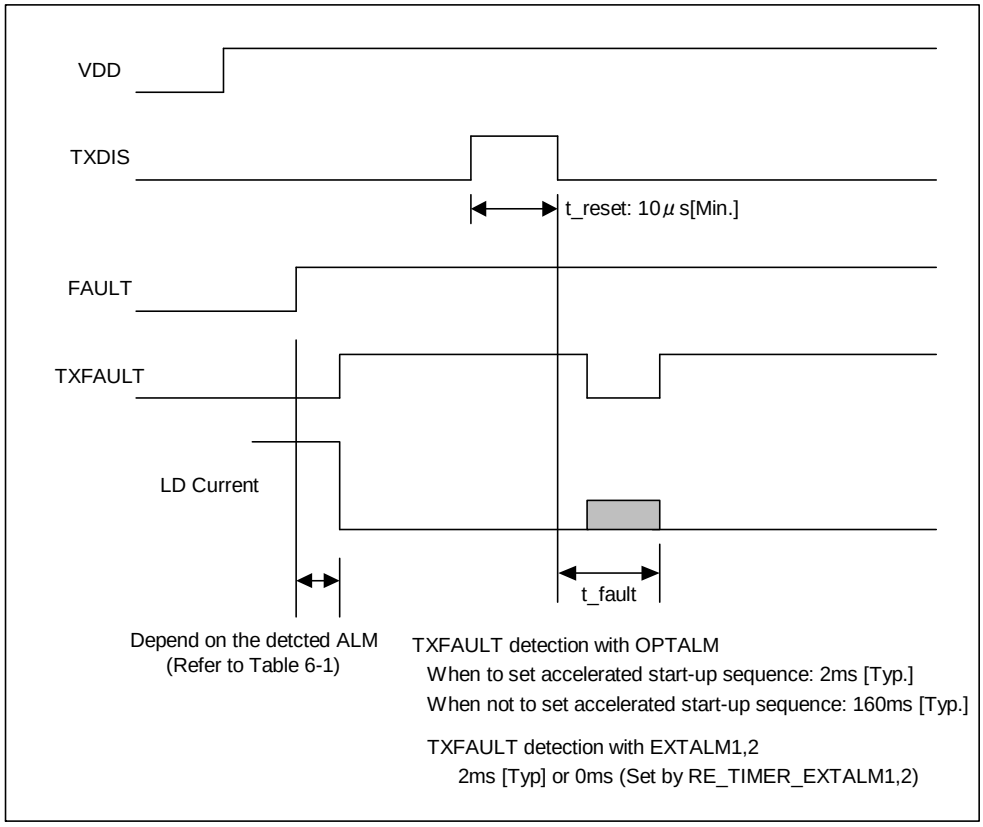


Figure 8-6 TXFAULT Detection / Release Sequence (When FAULT is not released)

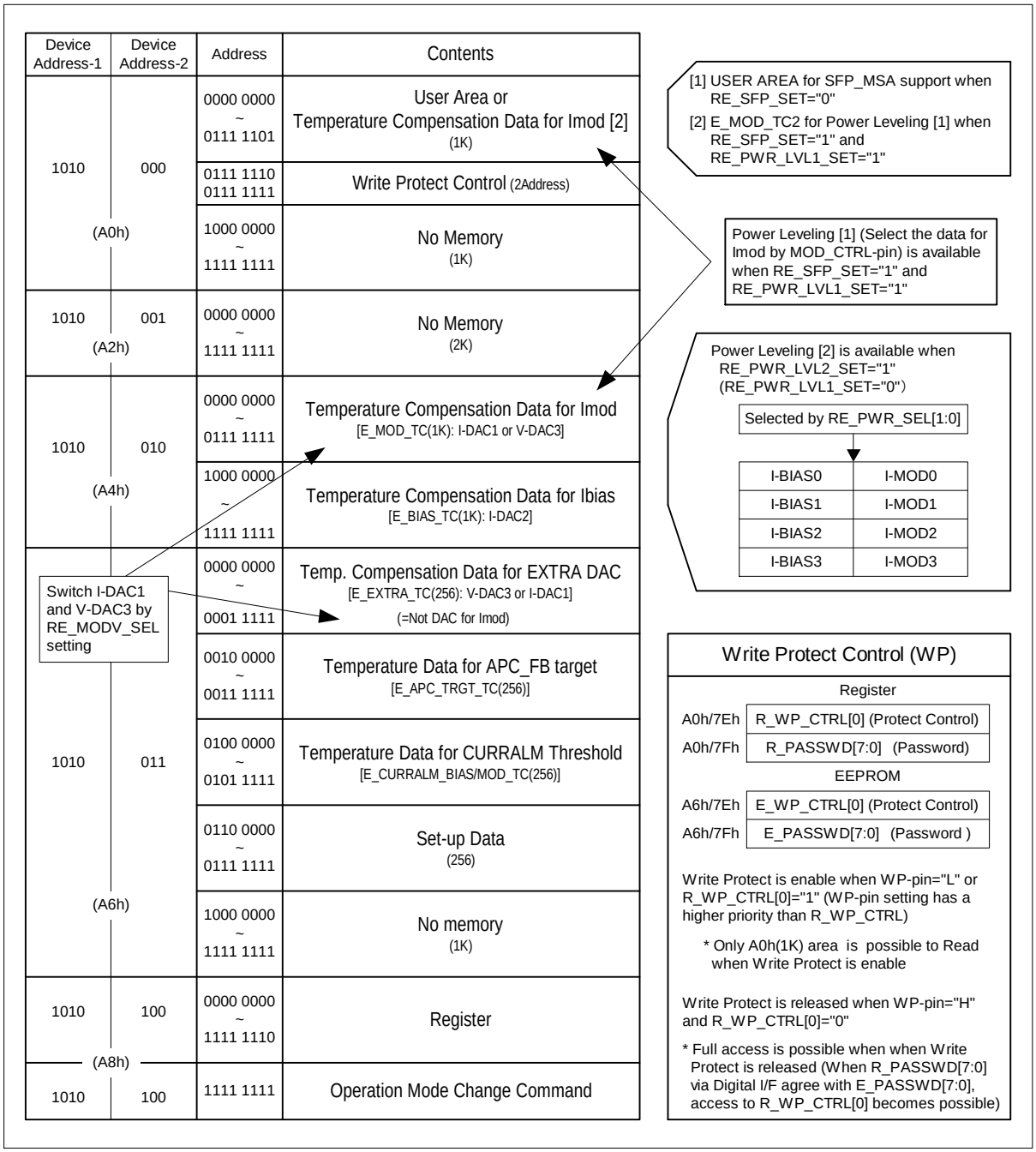


9. Digital Interface Configuration

9.1 Memory Configuration

EEPROM and Register configuration is shown in Figure 9-1. Access to EEPROM and Register is executed via 2-wire Digital Interface (I/F).

Figure 9-1 Memory Configuration



[*] Device address is configured with Device address-1 ("1010 "="Ah") and Device address-2.
Device address-2 in 3 bits Binary expression is converted into Hexadecimal code by multiplying it by 2.
For example, when Device address-1="1010" and Device address-2="011", Device address becomes "A6h".

9.2 Write Protect Operation

Accessible range and Device address via Digital I/F are determined by Write Protect setting as shown in Table 9-1.

Table 9-1 Write Protect Operation

Item	WP = "H"		WP = "L"
R_WP_CTRL	0	1	x
Device address	1010 xxx	1010 000	1010 000
ACK	When corresponding Device address is input via Digital I/F [*1]		
Access to EEPROM / Register	Full Access [*2]	A0h only Read only	A0h only Read only
Operation mode	Transition to any operation mode is possible	Self-Operation Mode only	Self-Operation Mode only
Page Write	Sequential write operation of EEPROM is possible in every 16 bytes. Sequential write operation of Register (Address after A8h/3Eh is folded back to A8h/00h).	—	—
Sequential Read	Sequential read operation of both EEPROM and Register is possible within the designated address area respectively. Address after A6h/FFh is folded back to A0h/00h in EEPROM and address after A8h/3Fh is folded back to A8h/00h in Register. "Non-actual space" address is not skipped.	Sequential read is possible in accessible EEPROM area.	

[*1] ACK signal is not returned during the writing operation into EEPROM.

[*2] When Write Protect is released (WP-pin="H" and R_WP_CTRL="0"), writing into R_PWR_SEL[1:0] at address = A8h / 2Fh is possible in Self-Operation Mode.

About Write Protect Setting

* The data for fully accessible setting (E_WP_CTRL="0", E_PASSWD="0") is programmed at AKM.

(a) Write Protect operation is "ON" when WP-pin at "L".
WP-pin setting has a higher priority than R_WP_CTRL (Register for Write Protect setting).

(b) Write Protect operation is controlled to be "ON " or "OFF" by R_WP_CTRL when WP-pin is at "H".
Access to R_WP_CTRL is possible only when R_PASSWD [7:0] (Register for Write Protect password), which is loaded via digital I/F, agrees with E_PASSWD [7:0] that is the password retained in advance.
Be noted that other than "00h" should be written into E_PASSWD [7:0] to enable Write Protect.

- R_WP_CTRL="0" → Full access is possible
- R_WP_CTRL="1" → Only the area in Device address='1010 000(A0h)' is accessible (Read Only), especially only Write Protect control register (R_PASSWD, R_WP_CTRL) are writable

Accordingly, when Self-Operation Mode is set by R_WP_CTRL="1", access to the adjusting data is executed as the following procedure,

(1) Make it enable to access to R_WP_CTRL by setting the same value to R_PASSWD as is retained in E_PASSWD in advance.
(2) Set R_WP_CTRL= "0" to enable full access.
(3) When to modify EEPROM content, shift the mode into EEPROM Access Mode and then modify data.

At the Power-on or when Self-Operation Mode is set, R_PASSWD is reset to "00h" and E_WP_CTRL value is loaded to R_WP_CTRL. So, if E_WP_CTRL is set to "0", Write Protect operation is automatically released at Power-on or when Self-Operation Mode is set.

Table 9-2 Write Protect Control Register / EEPROM

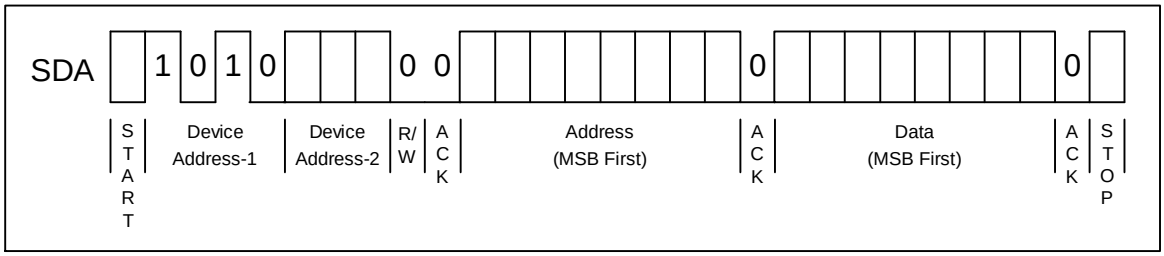
Register	EEPROM	D7	D6	D5	D4	D3	D2	D1	D0
A0h / 7Eh	A6h / 7Eh	—	—	—	—	—	—	—	WP_CTRL
A0h / 7Fh	A6h / 7Fh	PASSWD							

9.3 Read / Write Operation

9.3.1 Byte Write

Byte Write operation is shown in Figure 9-2. Select address and then input the data to be written.

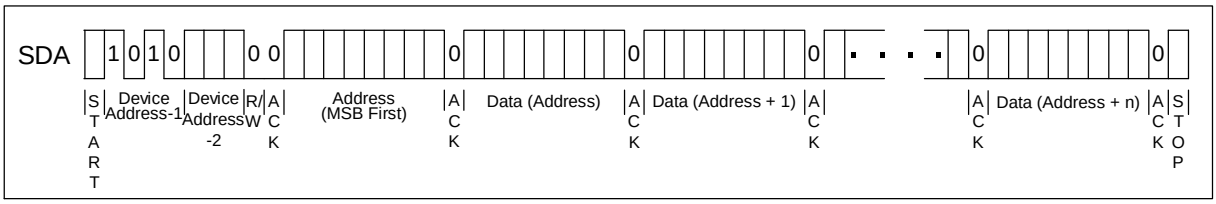
Figure 9-2 Byte Write



9.3.2 Page Write

Page Write operation is shown in Figure 9-3. Up to 16 bytes of data can be written at one time. In Page Write operation, the lower 4 bits of the 8 bits address are effective and the upper 4 bits data does not change. Therefore after writing data at "xxxx 1111", next address to be written is "xxxx 0000".

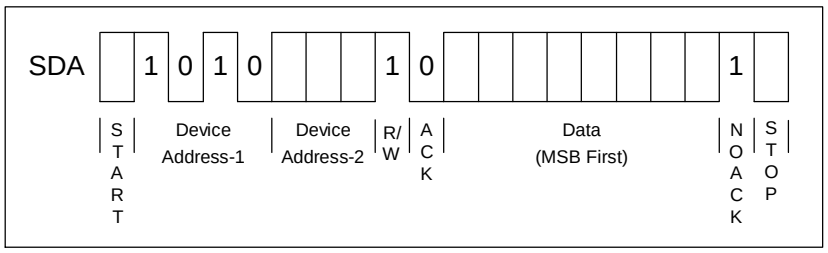
Figure 9-3 Page Write



9.3.3 Current Address Read

Current Address Read operation is shown in Figure 9-4. Address location where data is to be read out is "most recently accessed address + 1".

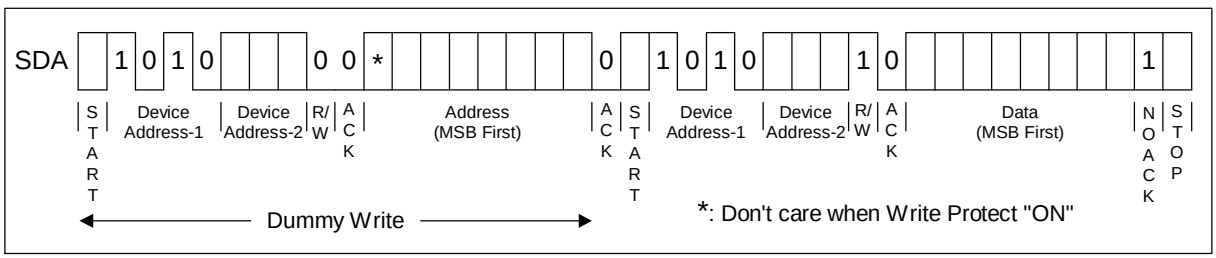
Figure 9-4 Current Address Read



9.3.4 Random Read

Random Read operation is shown in Figure 9-5. When to execute Random Read operation, assign an address to be read out by Dummy Write operation, and issue a Read instruction.

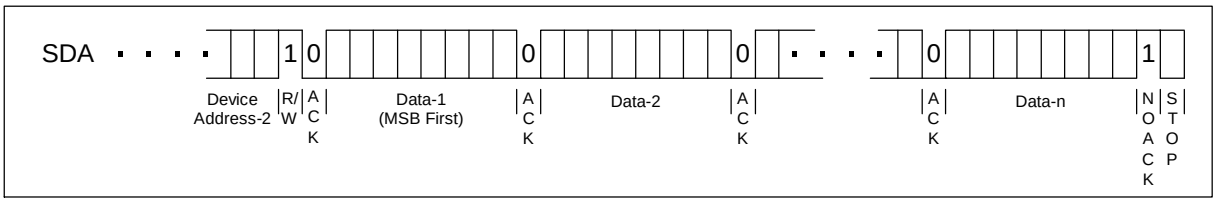
Figure 9-5 Random Read



9.3.5 Sequential Read

Sequential Read operation is shown in Figure 9-6. After the data at the designated address is output by read instruction, next address data can be read out if ACK signal is generated without stop bit signal that is sent from a master controller

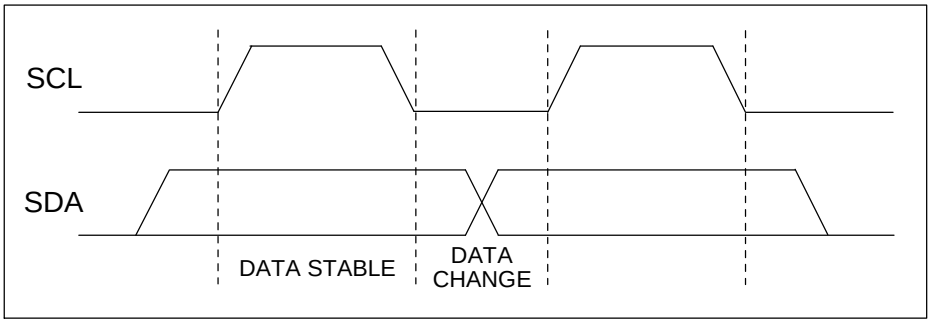
Figure 9-6 Sequential Read



9.3.6 Data Change

Data Change timing chart is shown in Figure 9-7. Data change (SDA) is made while SCL is at "L".

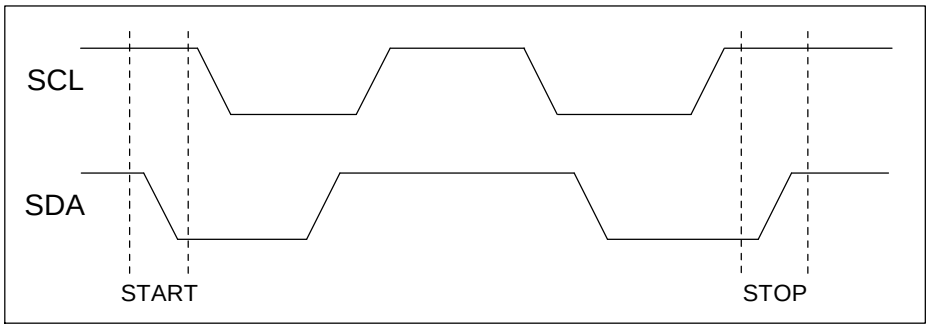
Figure 9-7 Data Change



9.3.7 Start / Stop

Start / Stop timing chart is shown in Figure 9-8. While SCL is at "H", Start is effective by setting SDA from "H" to "L", and Stop is effective by setting SDA from "L" to "H".

Figure 9-8 Start / Stop



9.4 EEPROM Configuration

EEPROM configuration is listed in Table 9-3. EEPROM configuration of adjustment data area is listed in Table 9-4 and Table 9-5. The access to EEPROM depends on its operation modes (Refer to Table 10-1). And the access to EEPROM is also limited by Write Protect setting (Refer to Section 9.2).

< Important Notice > The adjusted data in AKM factory are stored in advance at address location (Device Address=A6h, Address=60h) for the offset voltage of the On-chip temperature sensor. If such excessive temperature stress is to be applied to the AK2572 which exceeds a guaranteed EEPROM data retention conditions (for 10 years at 85℃), it is important to read the pre-determined data in advance and to re-write the same data back into EEPROM after an exposure to the excessive temperature environment. Even if the exposure time is shorter than the retention time, any accelerated temperature stress tests (such as baking) are performed, it is recommended to read the pre-set data first and to re-write it after the test. Access to unused address locations is not functionally guaranteed.

Table 9-3 EEPROM Address Configuration

Device Address	Address	Data (D7 ~ D0)	Initial value	Note
A0h	00h (0) ~ 7Dh (125)	User Area (1k bits)	00h	[*1]
A0h	80h (128) ~ FFh (255)	No Memory	—	
A2h	00h (0) ~ FFh (255)	No Memory	—	
A4h	00 h (0) ~ 7Fh (127)	E_MOD_TC (1k bits) Temperature Compensation Data for Imod	00h	[*2]~[*4]
A4h	80h (128) ~ FFh (255)	E_BIAS_TC (1k bits) Temperature Compensation Data for Ibias	00h	[*2], [*3]
A6h	00h (0) ~ 1Fh (31)	E_EXTRA_TC (256 bit) Temperature Compensation Data for EXTRA DAC	00h	[*5]
A6h	20h (32) ~ 3Fh (63)	E_APC_TRGT_TC (256 bit) Temperature Compensation Data for APC target	00h	[*5]
A6h	40h (64) ~ 5Fh (95)	E_CURRALM_BIAS / MOD_TC (256 bit) Temperature Compensation Data for CURRALM threshold	FFh	[*5]
A6h	60h (96) ~ 6Ah (106)	Adjustment Data (88 bit)	—	
A6h	6Bh (107) ~ 7Dh (125)	Reserved (152 bit)	—	
A6h	7Eh (126), 7Fh (127)	Write Protect Control (16 bit)	00h	

[*1] With both RE_SFP_SET = "1" and RE_PWR_LVL1 = "1", this area becomes setting area for Imod temperature compensation data [2] (E_MOD_TC2) of Power Leveling [1] function.

[*2] R_TEMP (Upper 7 bits A-to-D code of the temperature sensor) and address are corresponded (1.5 ℃/step) and then the temperature compensation data is written.

[*3] With RE_PWR_LVL1="0" and RE_PWR_LVL2="1", these area become setting area for Ibias and Imod temperature compensation data of Power Leveling [2] function.

[*4] With both RE_SFP_SET = "1" and RE_PWR_LVL1 = "1", this area becomes setting area for Imod temperature compensation data [1] (E_MOD_TC1) of Power Leveling [1] function.

[*5] Upper 5 bits of R_TEMP and address are corresponded (6.0 ℃/step), and then the temperature compensation data is written.

Table 9-4 EEPROM : Adjustment Data Configuration

EEPROM	Address	Function	Bit	Initial	Note
E_VREFTRIM [7:4]	60h	On-chip oscillator frequency	4	Factory setting	
E_TEMP _OFFSET [3:0]	60h	Temperature sensor offset	4	Factory setting	
E_PWR_SEL [7:6]	61h	EEPROM data switching at Power Leveling [2]	2	0	Refer to Table 5-2
E_BURST_ALM [5:4]	61h	EXTALM mask setting at Burst mode	2	0	0:Non-masked, 1:Masked [5]: EXTALM2, [4]: EXTALM1
E_BURST_SET [3]	61h	Burst mode setting	1	0	0:OFF, 1:ON
E_PWR_LVL2 _SET [2]	61h	Power Leveling [2] setting	1	0	0:OFF, 1:ON
E_SFP_SET [1]	61h	SFP_MSA support setting	1	0	0:ON, 1:OFF
E_PWR_LVL1_SET [0]	61h	Power Leveling [1] setting	1	0	Refer to Table 5-1
E_APC_FF_SET [7:6]	62h	APC FF setting	2	0	Refer to Table 4-6
E_APC_FB_SET [5:4]	62h	APC FB setting	2	0	Refer to Table 4-6
E_APC_INIT_SET [3]	62h	APC_FB initial value setting	1	0	0: OFF, 1: ON
E_DAC3_GAIN [2]	62h	V-DAC3 gain setting	1	0	0:Gain＝1, 1:Gain＝1.2/2.2
E_DAC2_GAIN [1]	62h	I-DAC2 gain setting	1	0	0:Gain＝1/2, 1: Gain＝1
E_DAC1_GAIN [0]	62h	I-DAC1 gain setting	1	0	0:Gain＝1/10, 1: Gain＝1
E_TIMER _OPTALM [6]	63h	OPTALM mask time setting for SFP_TXFAULT detection	1	0	0:160ms, 1:2ms [Typ.] (Refer to Table 8-1)
E_EXTALM2_POL [5]	63h	EXTALM2 polarity setting	1	0	0:“H” active, 1:“L” active
E_EXTALM1_POL [4]	63h	EXTALM1 polarity setting	1	0	0:“H” active, 1:“L” active
E_TEMP_DET [3]	63h	Temperature difference detection at Shutdown release	1	0	0:OFF, 1:ON Refer to Section 7.2
E_DAC_SET [2:0]	63h	DAC operation setting	3	0	0:OFF, 1:ON [2]: V-DAC3, [1]: I-DAC2 [0]: I-DAC1
E_OPTALM [7:6]	64h	OPTALM threshold	2	0	0 : 1/3, 1: 1/4, 2 : 1/6, 3 : 1/7
E_PDGAIN [5:0]	64h	PD gain setting	6	00h	Refer to Table 4-3
E_EXTALM2_SET [5]	65h	EXTALM2 setting for TXFAULT	1	0	0:OFF, 1:ON (Target)
E_EXTALM1_SET [4]	65h	EXTALM1 setting for TXFAULT	1	0	0:OFF, 1: ON (Target)
E_CURRALM_SET [3]	65h	CURRALM setting for TXFAULT	1	0	0:OFF, 1: ON (Target)
E_OPTALM_SET [2]	65h	OPTALM setting for TXFAULT	1	0	0:OFF, 1: ON (Target)
E_TIMER _EXTALM2 [1]	65h	EXTALM2 mask time setting for SFP_TXFAULT detection	1	0	0:0ms , 1:2ms [Typ.] （Refer to Table 8-2）
E_TIMER _EXTALM1 [0]	65h	EXTALM1 mask time setting for SFP_TXFAULT detection	1	0	0:0ms , 1:2ms [Typ.] （Refer to Table 8-2）
E_TEMPALM_SET [7]	66h	TEMPALM setting for TXFAULT	1	0	0:OFF, 1: ON (Target)
E_TEMP_WIN [7:0]	67h	Window setting for Temperature difference detection	8	00h	Refer to Section 7.2 and Table 4-10
E_MODV_SEL [7]	68h	DAC setting for Imod (Data setting for I-DAC1,V-DAC3)	1	0	Refer toTable 3-4
E_MOD_FBRT [6:0]	68h	APC_FB dividing value for Imod	7	00h	Refer to Section 4.2.4
E_BIAS_FBRT [6:0]	69h	APC_FB dividing value for Ibias	7	00h	Refer to Section 4.2.4
E_TEMPALM [7:0]	6Ah	TEMPALM threshold	8	00h	Refer toTable 4-10

Table 9-5 EEPROM : Adjustment Data Setting Map ("0" must be written where data bit is marked with "0")

Address	D7	D6	D5	D4	D3	D2	D1	D0
60h	VREFTRIM				TEMP_OFFSET			
61h	PWR_SEL		BURST_ALM		BURST _SET	PWR_LVL2 _SET	SFP_SET	PWR_LVL1 _SET
62h	APC_FF_SET		APC_FB_SET		APC_INIT _SET	DAC3 _GAIN	DAC2 _GAIN	DAC1 _GAIN
63h	0	TIMER_ OPTALM	EXTALM2 _POL	EXTALM1 _POL	TEMP _DET	DAC_SET		
64h	OPTALM		PDGAIN					
65h	0	0	EXTALM2 _SET	EXTALM1 _SET	CURRALM _SET	OPTALM _SET	TIMER_ EXTALM2	TIMER_ EXTALM1
66h	TEMPALM _SET	0	0	0	0	0	0	0
67h	TEMP_WIN							
68h	MODV _SEL	MOD_FBRT						
69h	—	BIAS_FBRT						
6Ah	TEMPALM							

9.5 Register Configuration

In Table 9-6 and Table 9-7, Register configuration is shown. As to the access limitations via Digital I/F, please refer to Table 9-1. Details of " R/W " column and " Form " column in Table 9-6 are described below.

(1) "R/W" column

R : Read only operation is possible in Adjustment Mode and in Self-Operation Mode when Write Protect operation is released. Writing the data into these Registers via Digital I/F is impossible.

R/W : Read / Write operation is possible in Adjustment Mode, and Read operation is possible in Self-Operation Mode when Write Protect operation is released.
Data written via Digital I/F is retained till operation mode is altered or data is modified. The AK2572 allows LD module adjustment at the product shipment by modifying the data in R/W registers.

R/FW: In addition to R/W function above, Read / Write operation is possible in Self-Operation Mode when Write Protect operation is released.

(2) "Form" column

U : Unsigned S : Signed (2's Complement)

Table 9-6 Register Configuration

Register	Address	Function	Bit	Form	R/W	Note
R_VREFTRIM [7:4]	00h	On-chip oscillator frequency	4	U	R/W	
R_TEMP _OFFSET [3:0]	00h	Temperature sensor offset	4	U	R/W	
R_PWR_SEL [7:6]	01h	EEPROM data switching at Power Leveling [2]	2	U	R/W	Refer to Table 5-2 [*1]
R _BURST_ALM [5:4]	01h	EXTALM mask setting at Burst mode	2	U	R/W	0:Non-masked, 1:Masked [5]: EXTALM2, [4]: EXTALM1
R _BURST_SET [3]	01h	Burst mode setting	1	U	R/W	0:OFF, 1:ON
R_PWR_LVL2 _SET [2]	01h	Power Leveling [2] setting	1	U	R/W	0:OFF, 1:ON
R_SFP_SET [1]	01h	SFP_MSA support setting	1	U	R/W	0:ON, 1:OFF
R_PWR_LVL1_SET [0]	01h	Power Leveling [1] setting	1	U	R/W	Refer to Table 5-1

Table 9-6 Register Configuration (Continued)

Register	Address	Function	Bit	Form	R/W	Note
R_APC_FF_SET [7:6]	02h	APC FF setting	2	U	R/W	Refer to Table 4-6
R_APC_FB_SET [5:4]	02h	APC FB setting	2	U	R/W	Refer to Table 4-6
R_APC_INIT_SET [3]	02h	APC_FB initial value setting	1	U	R/W	0: OFF, 1: ON
R_DAC3_GAIN [2]	02h	V-DAC3 gain setting	1	U	R/W	0:Gain＝1 1:Gain＝1.2/2.2
R_DAC2_GAIN [1]	02h	I-DAC2 gain setting	1	U	R/W	0:Gain＝1/2, 1: Gain＝1
R_DAC1_GAIN [0]	02h	I-DAC1 gain setting	1	U	R/W	0:Gain＝1/10, 1: Gain＝1
R_TIMER _OPTALM [6]	03h	OPTALM mask time setting for SFP_TXFAULT detection	1	U	R/W	0:160ms, 1:2ms [Typ.] (Refer to Table 8-1)
R_EXTALM2_POL [5]	03h	EXTALM2 polarity setting	1	U	R/W	0:“H” active, 1:“L” active
R_EXTALM1_POL [4]	03h	EXTALM1 polarity setting	1	U	R/W	0:“H” active, 1:“L” active
R_TEMP_DET [3]	03h	Temperature difference detection at Shutdown release	1	U	R/W	0:OFF, 1:ON Refer to Section 7.2
R_DAC_SET [2:0]	03h	DAC operation setting	3	U	R/W	0:OFF, 1:ON [2] : V-DAC3, [1] : I-DAC2 [0] : I-DAC1
R_OPTALM [7:6]	04h	OPTALM threshold	2	U	R/W	0:1/3, 1:1/4, 2:1/6, 3:1/7
R_PDGAIN [5:0]	04h	PD gain setting	6	U	R/W	Refer to Table 4-3
R_EXTALM2_SET [5]	05h	EXTALM2 setting for TXFAULT	1	U	R/W	0:OFF, 1:ON (Target)
R_EXTALM1_SET [4]	05h	EXTALM1 setting for TXFAULT	1	U	R/W	0:OFF, 1: ON (Target)
R_CURRALM_SET [3]	05h	CURRALM setting for TXFAULT	1	U	R/W	0:OFF, 1: ON (Target)
R_OPTALM_SET [2]	05h	OPTALM setting for TXFAULT	1	U	R/W	0:OFF, 1: ON (Target)
R_TIMER _EXTALM2 [1]	05h	EXTALM2 mask time setting for SFP_TXFAULT detection	1	U	R/W	0:0ms , 1:2ms [Typ.] （Refer to Table 8-2）
R_TIMER _EXTALM1 [0]	05h	EXTALM1 mask time setting for SFP_TXFAULT detection	1	U	R/W	0:0ms , 1:2ms [Typ.] （Refer to Table 8-2）
R_TEMPALM_SET [7]	06h	Set TEMPALM for TXFAULT	1	U	R/W	0:OFF, 1: ON (Target)
R_TEMP_WIN [7:0]	07h	Window setting for Temperature difference detection	8	U	R/W	Refer to Section 7.2 and Table 4-10
R _MODV_SEL [7]	08h	DAC setting for Imod (Data setting for I-DAC1, V-DAC3)	1	U	R/W	Refer to Table 3-4
R_MOD_FBRT [6:0]	08h	APC_FB dividing value for Imod	7	U	R/W	Refer to Section 4.2.4
R_BIAS_FBRT [6:0]	09h	APC_FB dividing value for Ibias	7	U	R/W	Refer to Section 4.2.4
R_APC_FBIV [7:0]	0Ah	APC FB initial value	8	U	R/W	Refer to Table 4-10 [*2]
R_APC_TRGT [4:0]	0Bh	APC target setting	5	U	R/W	Refer to Table 4-4
R_MOD_FF [7:0]	0Ch	APC_FF value for Imod	8	U	R/W	I-DAC1 or V-DAC3
R_BIAS_FF [7:0]	0Dh	APC_FF value for Ibias	8	U	R/W	I-DAC2
R_EXTRA [7:0]	0Eh	EXTRA DAC value	8	U	R/W	V-DAC3 or I-DAC1 (DAC isn’t for Imod)
R_CURRALM _BIAS [7:4]	0Fh	CURRALM setting for Ibias	4	U	R/W	Refer to Section 6.3
R_CURRALM _MOD [3:0]	0Fh	CURRALM setting for Imod	4	U	R/W	Refer to Section 6.3

Table 9-6 Register Configuration (Continued)

Register	Address	Function	Bit	Form	R/W	Note
R_TEMP [7:0]	10h	Temperature equivalent value (AD code of temperature sensor)	8	U	R	Refer to Table 4-10
R_TEMP _STDW [7:0]	14h	Temperature equivalent value at just before Shutdown request	8	U	R	Refer to Section 7.2 and Table 4-10
R_TXFLT_ST [4:0]	19h	Alarm status	5	U	R	1: Active, 0: Inactive [4] TEMPALM [3] EXTALM2 [2] EXTALM1 [1] CURRALM [0] OPTALM
R_DAC1 [7:0]	1Bh	I-DAC1 value	8	U	R	[*3]
R_DAC2 [7:0]	1Ch	I-DAC2 value	8	U	R	[*3]
R_DAC3 [7:0]	1Dh	V-DAC3 value	8	U	R	[*3]
R_APC_FB [7:0]	1Eh	APC_FB value	8	S	R	[7]Sign of APC_FB [*2] [6:0] Upper 7bits of APC_FB
R_MODE [2:0]	1Fh	Operation mode	3	U	R	001:Self-Operation Mode 010:Adjustment Mode 100:EEPROM Access Mode
AKM test	28h~2Bh 2Eh	For AKM test	—	—	—	
R_PWR _SEL [1:0]	2Fh	EEPROM data switching at Power Leveling [2]	2	U	R/FW	Refer to Table 5-2 [*1]

[*1] Finally modified value in either R_PWR_SEL [7:6] (R/W) at address "01h" or R_PWR_SEL [1:0] (R/FW) at address "2Fh" becomes valid R_PWR_SEL set value and is updated and retained in R_PWR_SEL at both address locations. And with R_PWR_LVL1_SET="0" and R_PWR_LVL2_SET="1", Power Leveling[2] is available and write in Self-Operation Mode can be executable only to R_PWR_SEL [1:0] (R/WF) at address "2Fh" when Write Protect operation is released.

[*2] Data configuration is shown in Figure 9-9. Register is configured with the signed 9 bits data, but Read / Write operation via Digital I/F is processed in 8 bits configuration.

[*3] In Bias current setting DAC and Modulation current setting DAC, Digital code for DAC is given as following equation and negative value at R_DACx is set to "0".

R_DACx=R_DACx_FF+R_DACx_FB (x=1 ~ 3)

Figure 9-9 Signed Register Configuration

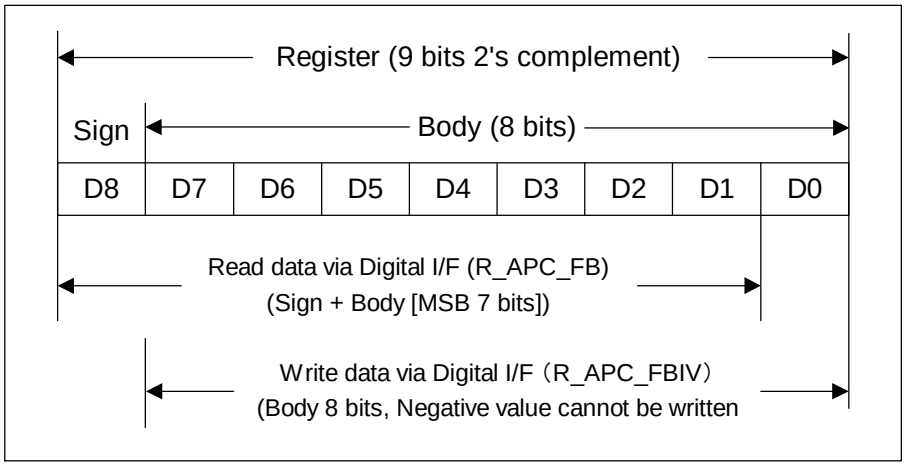


Table 9-7 Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0
00h	VREFTRIM				TEMP_OFFSET			
01h	PWR_SEL		BURST_ALM		BURST _SET	PWR_LVL2 _SET	SFP_SET	PWR_LVL1 _SET
02h	APC_FF_SET		APC_FB_SET		APC_INIT _SET	DAC3 _GAIN	DAC2 _GAIN	DAC1 _GAIN
03h	0	TIMER_ OPTALM	EXTALM2 _POL	EXTALM1 _POL	TEMP _DET	DAC_SET		
04h	OPTALM		PDGAIN					
05h	0	0	EXTALM2 _SET	EXTALM1 _SET	CURRALM _SET	OPTALM _SET	TIMER_ EXTALM2	TIMER_ EXTALM1
06h	TEMPALM _SET	0	0	0	0	0	0	0
07h	TEMP_WIN							
08h	MODV _SEL	MOD_FBRT						
09h	–	BIAS_FBRT						
0Ah	APC_FBIV							
0Bh	–	–	–	APC_TRGT				
0Ch	MOD_FF							
0Dh	BIAS_FF							
0Eh	EXTRA							
0Fh	CURRALM_BIAS				CURRALM_MOD			
10h	TEMP							
11h ~13h	–	–	–	–	–	–	–	–
14h	TEMP_STDW							
15h ~ 18h	–	–	–	–	–	–	–	–
19h				TXFLT_ST				
1Ah	STATUS							
1Bh	DAC1							
1Ch	DAC2							
1Dh	DAC3							
1Eh	R_APC_FB [8:1]							
1Fh	–	–	–	–	–	MODE		
20h ~ 27h	–	–	–	–	–	–	–	–
28h ~ 2Bh	Reserved (For AKM test)							
2Ch 2Dh	–	–	–	–	–	–	–	–
2Eh	Reserved (For AKM test)							
2Fh	–	–	–	–	–	–	PWR_SEL	

10. Operation Modes

The AK2572 has the following 3 operation modes – Self-Operation Mode where temperature compensation operation is automatically executed in accordance with EEPROM setting, Adjustment Mode where each LD adjustment is made and EEPROM Access Mode where adjusting data is written into EEPROM.

10.1 Self-Operation Mode

With the On-chip oscillator, those functions as temperature detection, read out of temperature compensation data from EEPROM and LD drive current setting by APC control, are automatically executed. At the Power-on, the AK2572 is put into Self-Operation Mode.

10.2 Adjustment Mode

This is a mode to adjust each LD characteristic. When the device is put into this mode, the temperature compensation operation stops and various setting data can be written via Digital I/F. Adjustment is made by accessing the internal Register via Digital I/F.

10.3 EEPROM Access Mode

This is a mode to write LD adjusting data and various set-up data into EEPROM.

10.4 Mode Control

In Figure 10-1, "Mode Transition Flow Chart" is shown. Transition to each mode is controlled by some commands (Refer to Section 10.5) via Digital I/F. Access to Digital I/F is prohibited for 2 msec [Typ.] after the transition to Self-Operation Mode is made (After the Power-on and after issuing Operation mode change command). Accessible EEPROM / Register via Digital I/F in each operation mode is listed in Table 10-1.

Figure 10-1 Mode Transition Flow Chart

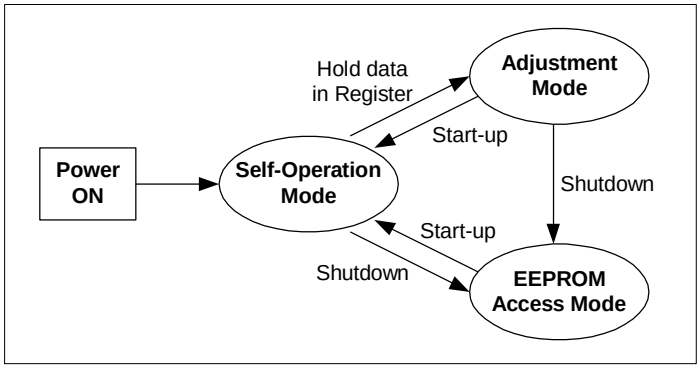


Table 10-1 Operational Conditions in Each Mode

WP-pin	R_WP_CTRL [*1]	Operation mode	EEPROM		Register	
			Read	Write	Read	Write
L	–	Fixed at Self-Operation Mode	○ [*2]	×	×	×
H	1	Fixed at Self-Operation Mode	○ [*2]	×	×	× [*1]
	0 [*4]	Self-Operation Mode	○	×	○	× [*1][*3][*5]
		Adjustment Mode	○	×	○	○ [*5] [*6]
		EEPROM Access Mode	○	○	×	× [*5]

[*1] If WP-pin="H", writing into R_PASSWD is always possible in Self-Operation Mode. When R_PASSWD and E_PASSWD agree, writing into R_WP_CTRL becomes possible.

[*2] When Write Protect is enabled (WP-pin="L" or R_WP_CTRL="1"), Self-Operation Mode is set as the operating mode and Read Only operation is possible at Device Address="A0h".

[*3] When Write Protect is released, writing into R_PWR_SEL[1:0] at Address="A8h / 2Fh" in Self-Operation Mode is possible. Power Leveling[2] is enabled at R_PWR_LVL1_SET="0"、R_PWR_LVL2_SET="1".

[*4] Full access is possible when Write Protect is released (WP-pin="H" and R_WP_CTRL="0").

[*5] "Operation Mode Change command " can be executed.

[*6] In Adjustment Mode, when R_SFP_SET is modified, the access via Digital I/F cannot be made for 80 msec [Typ.] from the data modification.

10.5 Operation Mode Change Commands

Transition to each mode is made by Operation Mode Change command via Digital I/F.
In Table 10-2, a list of Operation Mode Change commands is shown.

Table 10-2 Operation Mode Change Commands

Device Address	R/W	Address	Data	Operation mode set by command
1010 100	W	1111 1111	1010 0000	Self-Operation Mode
1010 100	W	1111 1111	1010 0111	Adjustment Mode
1010 100	W	1111 1111	1010 1110	EEPROM Access Mode

10.6 Mode Protection

In order to protect from shifting into Adjustment Mode or EEPROM Access Mode due to un-expected external hazard such as noise during Self-Operation Mode, WP-pin = “L” or R_WP_CTRL＝“1” should be set to inhibit the above erroneous operation.

11. Example of Adjusting Sequence

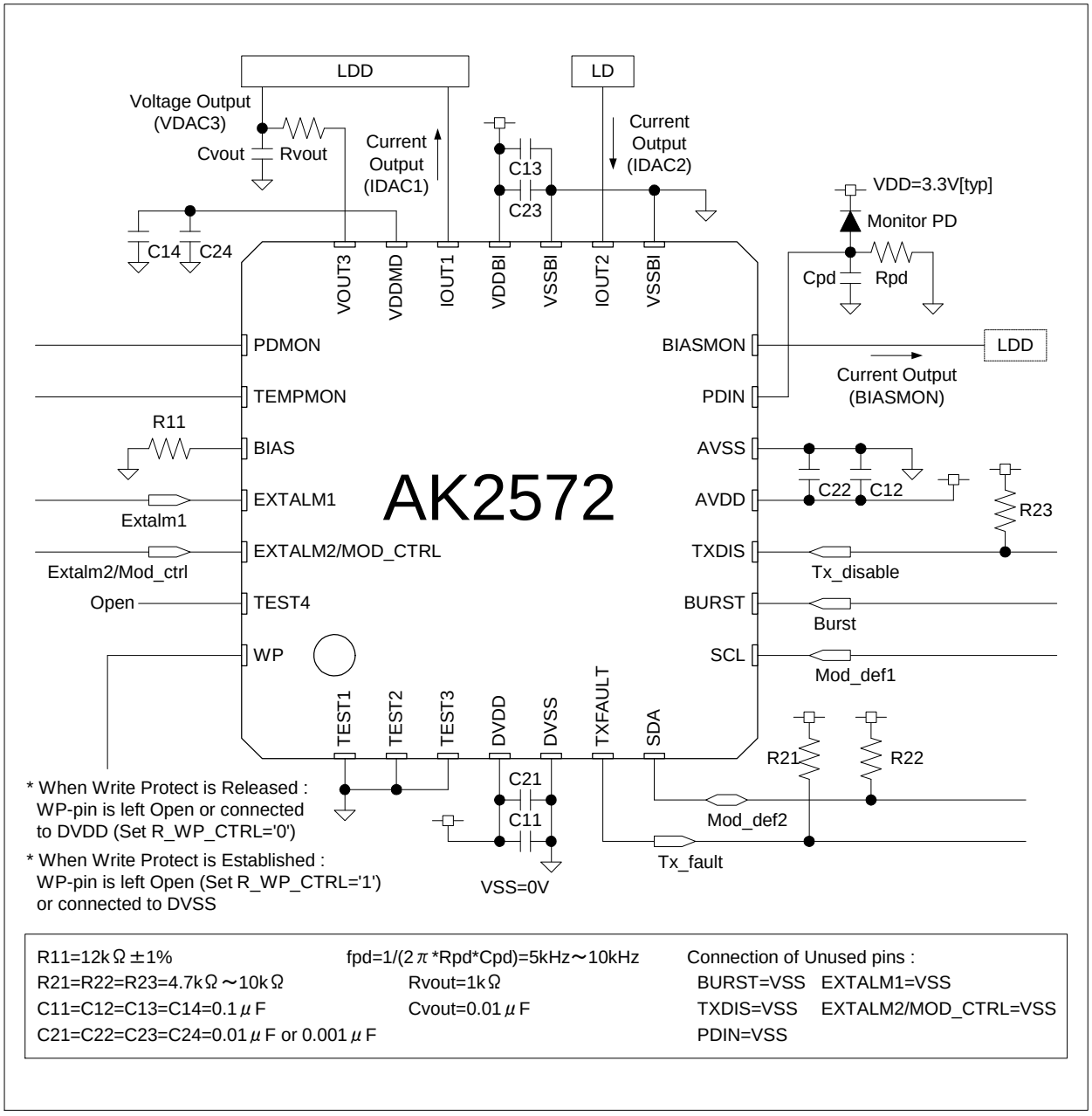
Adjusting sequence example is shown in Table 11-1.

Table 11-1 Example of Adjusting Sequence (for Continuous mode)

	Item	Contents
1	Transition to Adjustment Mode	After releasing the Write Protection, issue a command to make a transition into Adjustment Mode via Digital I/F.
2	Set APC_FB in open-loop operation	Set R_APC_FB_SET="0"、R_APC_FF_SET="3", and Bias current and Modulation current are set to open-loop operation. Output current range of I-DAC1 (or V-DAC3) for Modulation current and I-DAC2 for Bias current is set by R_DAC1_GAIN (or R_DAC3_GAIN) and R_DAC2_GAIN respectively.
3	LD power adjustment	Set R_MOD_FF (Modulation current) and R_BIAS_FF (Bias current) so that designated LD power is available.
4-A	PDGAIN adjustment (When to monitor PDMON-pin voltage)	Adjust PDMON-pin voltage when the designated LD power is output. Adjust PDMON-pin output voltage to be 1 [V] by R_PDGAIN. Set R_APC_TRGT (APC target)＝"1 0000" (its center value), and after making APC setting (R_APC_FB_SET, R_APC_FF_SET, R_MOD_FBRT and R_BIAS_FBRT when both Bias and Modulation currents are used for APC_FB setting), jump to "Step 5" in this table.
4-B	PDGAIN adjustment (When to monitor PDMON-pin voltage is impossible)	Set R_APC_TRGT (APC target)="1 0000" (its center value) and R_PDGAIN ＝ "00 0000" (23.5dB, Maximum gain), then make APC setting (R_APC_FB_SET, R_APC_FF_SET, R_MOD_FBRT and R_BIAS_FBRT when both Bias and Modulation currents are used for APC_FB setting), Then APC_FB function is activated and LD power is lowered. Adjust R_PDGAIN so that LD power reaches a closest amount to the designated power level, and jump to "Step 5" in this table.
5	APC_FB target adjustment	Adjust DAC_APC setting value (R_APC_TRGT) so that LD optical power reaches its designated power level.
6	Read-out of sensed temperature data	Read out the LSI chip-surface temperature equivalent value (R_TEMP).
7	Calculation of temperature characteristic	In order to adjust the temperature characteristic of LD, vary temperature and repeat "Steps 2 ~ 6" above when adjustment is made at 2 different temperature points or more and make the look-up table of I-DAC1 (or V-DAC3) and I-DAC2 with referring the measured data If the adjustment is executed at single temperature point, make the look-up table with the measured data and On-chip temperature sensor gain (1.5 ℃ /LSB [Typ.]).
8	Write the adjustment data into EEPROM	(1) Prepare the data to be written into EEPROM based on LD adjusting data. (2) Issue a command to make a transition into EEPROM Access Mode via Digital I/F. (3) Write adjusting data into EEPROM. (4) Verify that correct data is written, by reading out the written data.
9	Transition to Self-Operation Mode	After writing data into EEPROM, issue a command to make a transition to Self-Operation Mode via Digital I/F. Then the AK2572 automatically initiates its operation in accordance with the setting data retained in EEPROM.

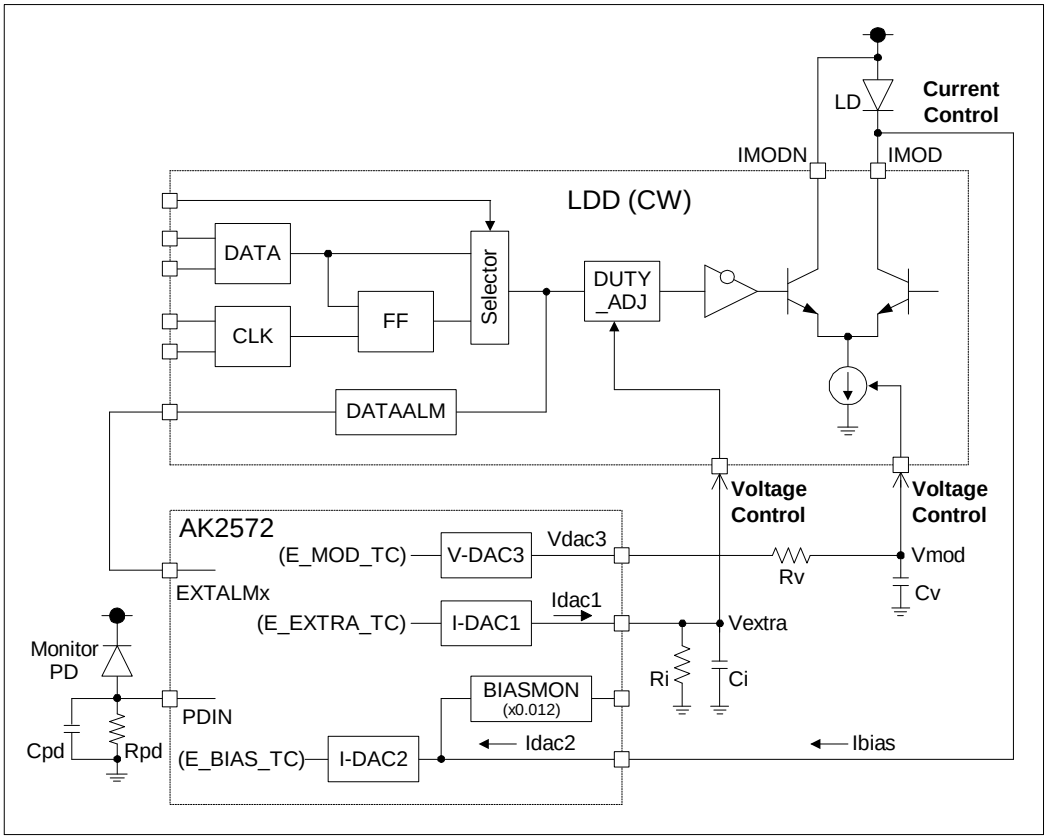
VI. EXTERNAL CIRCUIT EXAMPLE

Recommended External Circuit

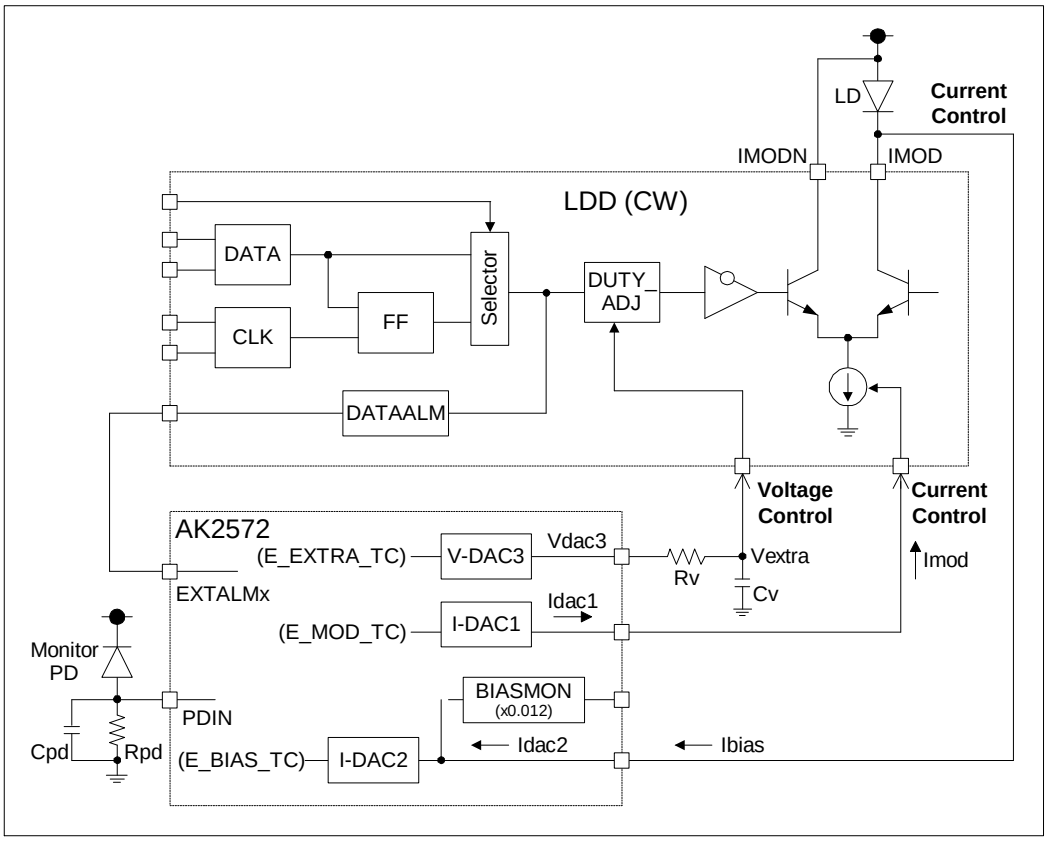


R11=12kΩ±1%	fpd=1/(2π*Rpd*Cpd)=5kHz～10kHz	Connection of Unused pins :
R21=R22=R23=4.7kΩ～10kΩ	Rvout=1kΩ	BURST=VSS EXTALM1=VSS
C11=C12=C13=C14=0.1μF	Cvout=0.01μF	TXDIS=VSS EXTALM2/MOD_CTRL=VSS
C21=C22=C23=C24=0.01μF or 0.001μF		PDIN=VSS

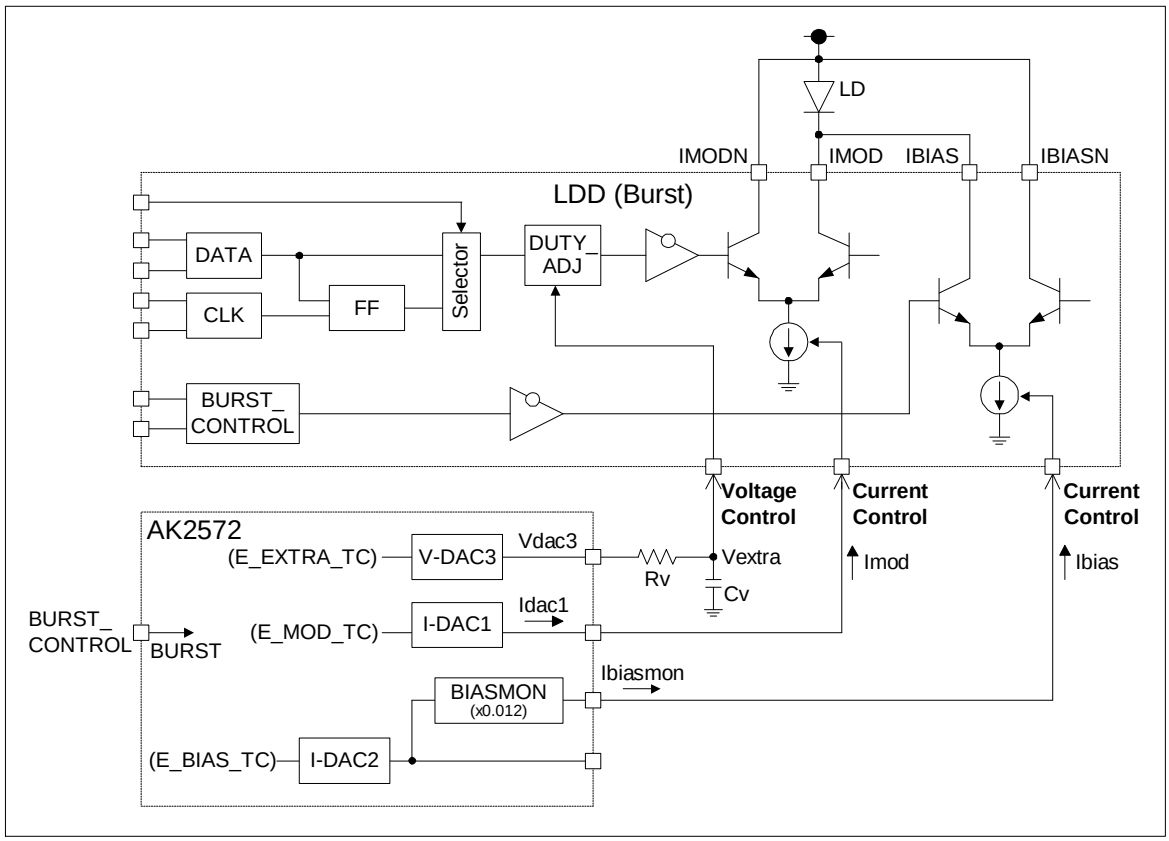
[A] Example of the connection to the LDD controlled by AK2572 voltage output for CW LD



[B] Example of the connection to the LDD controlled by AK2572 current output for CW LD



[C] Example of the connection to the LDD controlled by AK2572 current output for Burst transmission



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